MAINTENANCE MANUAL

FM/AM-1200
Communications Service Monitor

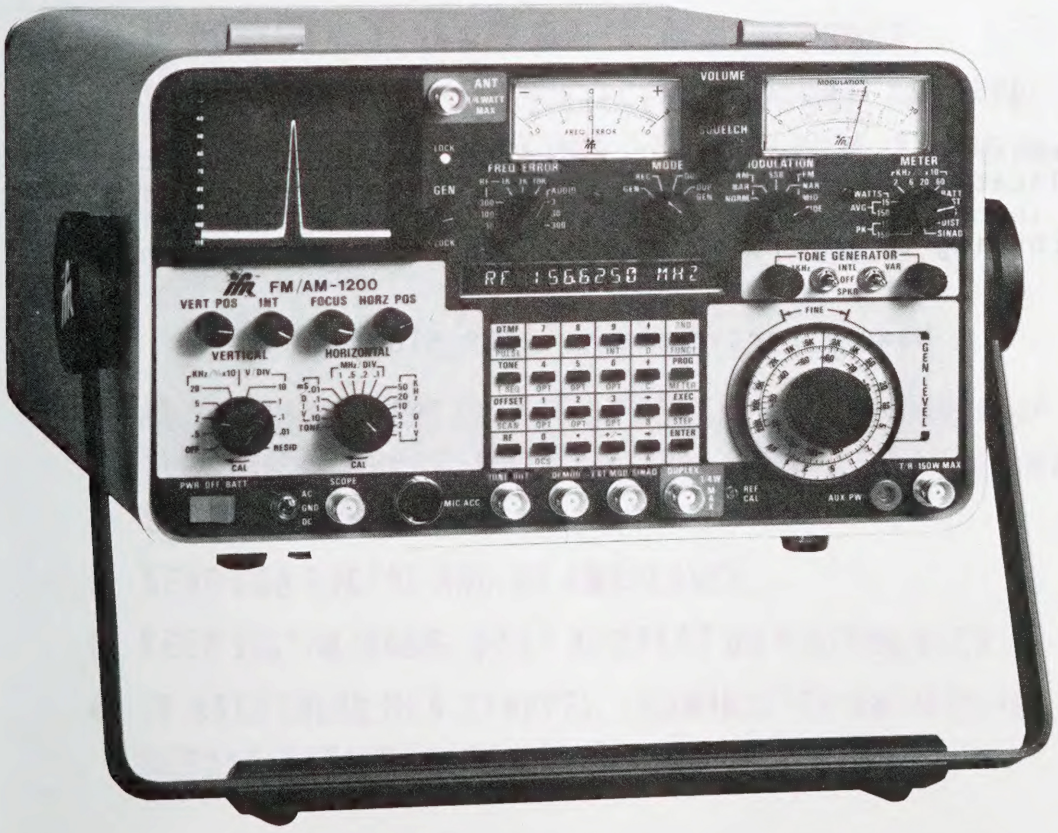


MP MASTER
MA30507

MAINTENANCE MANUAL

FM/AM-1200

COMMUNICATIONS SERVICE MONITOR



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Manual Part Number: 1002-5100-400

WARNING:

HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, A ROPE OR SOME OTHER DRY INSULATING MATERIAL.

FIRST AID

1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. SEND FOR DOCTOR AND/OR AMBULANCE.
3. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.
4. IF BREATHING HAS STOPPED , ADMINISTER ARTIFICIAL RESUSCITATION. STOP ALL SERIOUS BLEEDING.

CAUTION

INTEGRATED CIRCUITS AND SOLID STATE DEVICES SUCH AS MOS FET'S, ESPECIALLY CMOS TYPES, ARE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGES RECEIVED FROM IMPROPER HANDLING, THE USE OF UNGROUNDED TOOLS, AND IMPROPER STORAGE AND PACKAGING. ANY MAINTENANCE TO THIS UNIT MUST BE PERFORMED WITH THE FOLLOWING PRECAUTIONS:

1. BEFORE USE IN A CIRCUIT, KEEP ALL LEADS SHORTED TOGETHER EITHER BY THE USE OF VENDOR-SUPPLIED SHORTING SPRINGS OR BY INSERTING LEADS INTO A CONDUCTIVE MATERIAL.

2. WHEN REMOVING DEVICES FROM THEIR CONTAINERS, GROUND THE HAND BEING USED WITH A CONDUCTIVE WRISTBAND.

3. TIPS OF SOLDERING IRONS AND/OR ANY TOOLS USED MUST BE GROUNDED.

4. DEVICES MUST NEVER BE INSERTED INTO NOR REMOVED FROM CIRCUITS WITH POWER ON.

5. PC BOARD, WHEN TAKEN OUT OF THE SET, MUST BE LAID ON A GROUNDED CONDUCTIVE MAT OR STORED IN A CONDUCTIVE STORAGE BAG.

NOTE

Remove any built-in power source, such as a battery, before laying PC Boards on conductive mat or storing in conductive bag.

6. PC BOARDS, IF BEING SHIPPED TO THE FACTORY FOR REPAIR, MUST BE PACKAGED IN A CONDUCTIVE BAG AND PLACED IN A WELL-CUSHIONED SHIPPING BOX.

THE USE OF SIGNAL GENERATORS FOR MAINTENANCE AND OTHER ACTIVITIES CAN BE A SOURCE OF ELECTROMAGNETIC INTERFERENCE TO COMMUNICATION RECEIVERS, WHICH CAN CAUSE DISRUPTION AND INTERFERENCE TO COMMUNICATION SERVICE FOR A RADIUS OF SEVERAL MILES.

USERS OF THIS EQUIPMENT SHOULD SCRUTINIZE ANY OPERATION WHICH RESULTS IN RADIATION OF A SIGNAL (DIRECTLY OR INDIRECTLY) AND SHOULD TAKE NECESSARY PRECAUTIONS TO AVOID POTENTIAL COMMUNICATION INTERFERENCE PROBLEMS.

LIST OF EFFECTIVE PAGES

The manual pages listed below which are affected by a current change or revision, are so identified by a revision number and an asterisk.

Date of issue for original and changed pages are:

Original ..... 0 ..... September 1, 1985

TOTAL NUMBER OF PAGES IN THIS MANUAL IS 236 **CONSISTING OF FOLLOWING:**

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Warning Page	0
Caution Page	0
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B Blank	0
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3-1 thru 3-3	0
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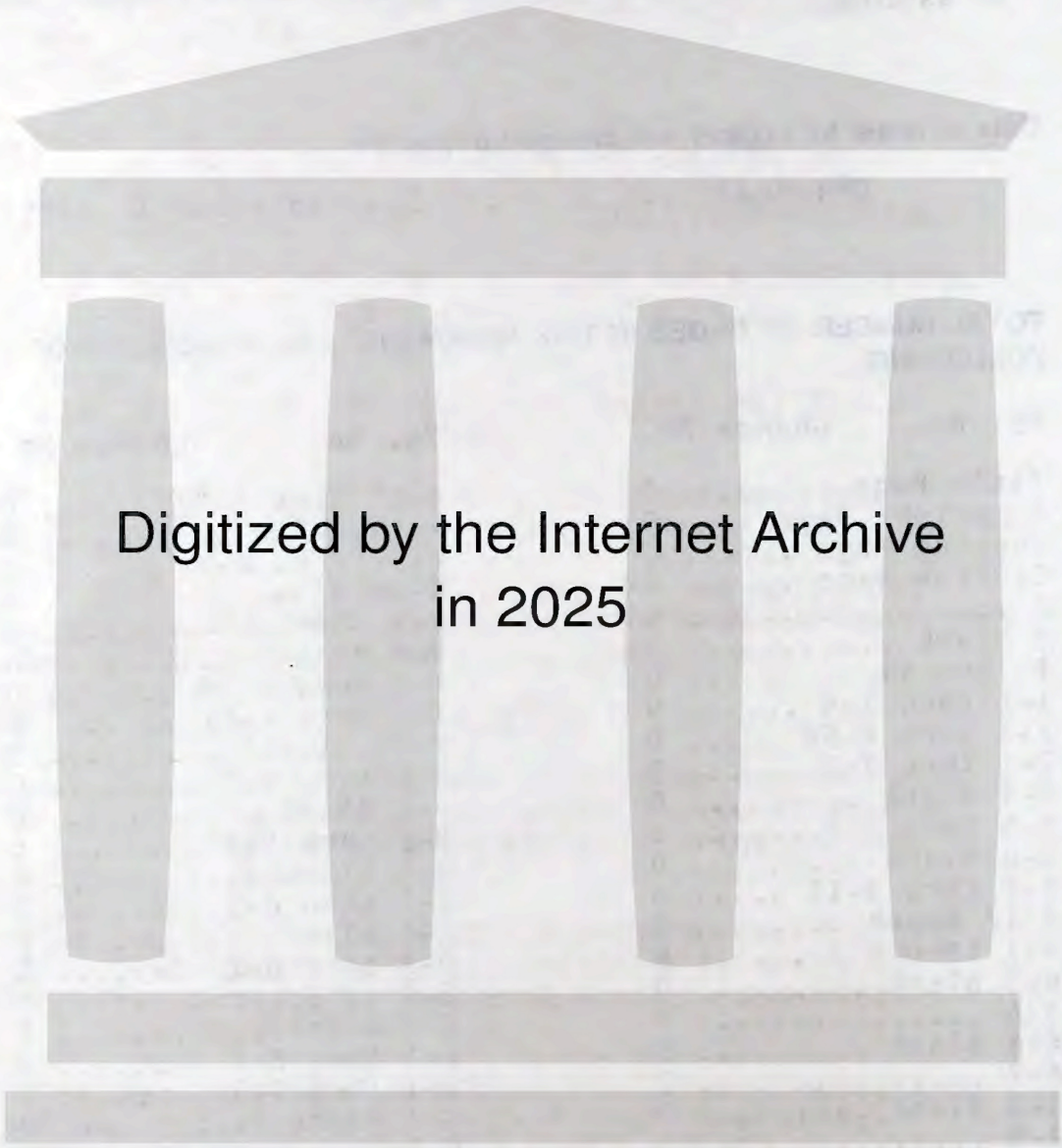

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PREFACE

SCOPE

This manual contains maintenance instructions for the FM/AM-1200 Communications Service Monitor. The information in this manual will enable the technician to:

1. Service, test, repair or replace any major assembly or module within the test set.
2. Maintain the operating condition of the set to expected performance standards.
3. Understand the principles of operation as they relate to the overall operation of the set as well as to individual circuits.

ORGANIZATION

The contents of this manual are divided into eight major sections:

SECTION 1 - INTRODUCTION

Provides a brief description of the electrical and mechanical configuration of the FM/AM-1200, intended to familiarize the technician with the overall structure of the set.

SECTION 2 - THEORY OF OPERATION

Describes the FM/AM-1200 circuit theory on three levels of complexity, a simplified overview, a functional theory of interactive modules, and a detailed theory of each module. Appropriate block diagrams accompany each discussion.

SECTION 3 - PERFORMANCE EVALUATION

Contains "covers on" functional checkout procedures for evaluating the performance of the FM/AM-1200 in each of its modes of operation and major functions.

SECTION 4 - CALIBRATION

Contains step-by-step calibration procedures for use at normal calibration intervals or after making repairs or replacements.

SECTION 5 - PREVENTIVE MAINTENANCE

Contains routine instructions for cleaning and inspection of the FM/AM-1200.

SECTION 6 - MECHANICAL ASSEMBLY DRAWINGS

Contains "exploded view" drawings of all mechanical assemblies within the FM/AM-1200 except PC Boards. Pertinent notes for disassembly and/or reassembly are included as required with individual drawings.

SECTION 7 - PC BOARD ASSEMBLIES/CIRCUIT SCHEMATICS

Contains component layout drawings for all PC Board assemblies, interconnect diagrams, circuit schematics, waveforms and charts reflecting voltage levels keyed to test points.

APPENDICES

Contains useful supplementary maintenance and operational data.

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SECTION 1 - INTRODUCTION

1-1 GENERAL

This section provides a brief description of the internal electrical and mechanical configurations of the FM/AM-1200, and will familiarize the technician with the overall structure of the set. FM/AM-1200 specifications are in Appendix A.

1-2 ELECTRICAL DESCRIPTION

The FM/AM-1200 is a processor controlled, digitally synthesized FM/AM/SSB receiver and generator, with an integral oscilloscope/ spectrum analyzer. The receiver is a triple conversion superheterodyne receiver capable of receiving signals from 250 kHz to 999.9999 MHz. The signal generator is capable of producing modulated or unmodulated RF signals from 250 kHz to 999.9999 MHz. A function generator will produce six functions with ranges from 10 Hz up to 10 kHz and one function up to 30 kHz. A duplex generator can produce a signal up to ±49.99 MHz from the received frequency. The oscilloscope and spectrum analyzer utilize a common CRT. Bandwidth of the oscilloscope is DC to 1 MHz and the dynamic range of the spectrum analyzer is from -30 dBm to -100 dBm.

1-2-1 FUNCTIONAL CONSTRUCTION

Individual modules which make up each function are listed below.

1. Power Supply

   Line Supply Assembly
   Inverter Assembly
   Battery Charger PC Board

2. Reference Frequencies

   Frequency Standard PC Board
   Standard or Optional TCXO or Optional Oven Oscillator
   Digital Module

3. Processor

   Processor PC Board
   Interface I/O PC Board
   DVM I/O PC Board
   Display PC Board
   Keyboard

4. Frequency Synthesizer

High Loop Assembly
Dual VCO Assembly
1120 MHz Low Pass Filter
High/Low Pass Filter
Low Loop Assembly

5. Receive/Generate

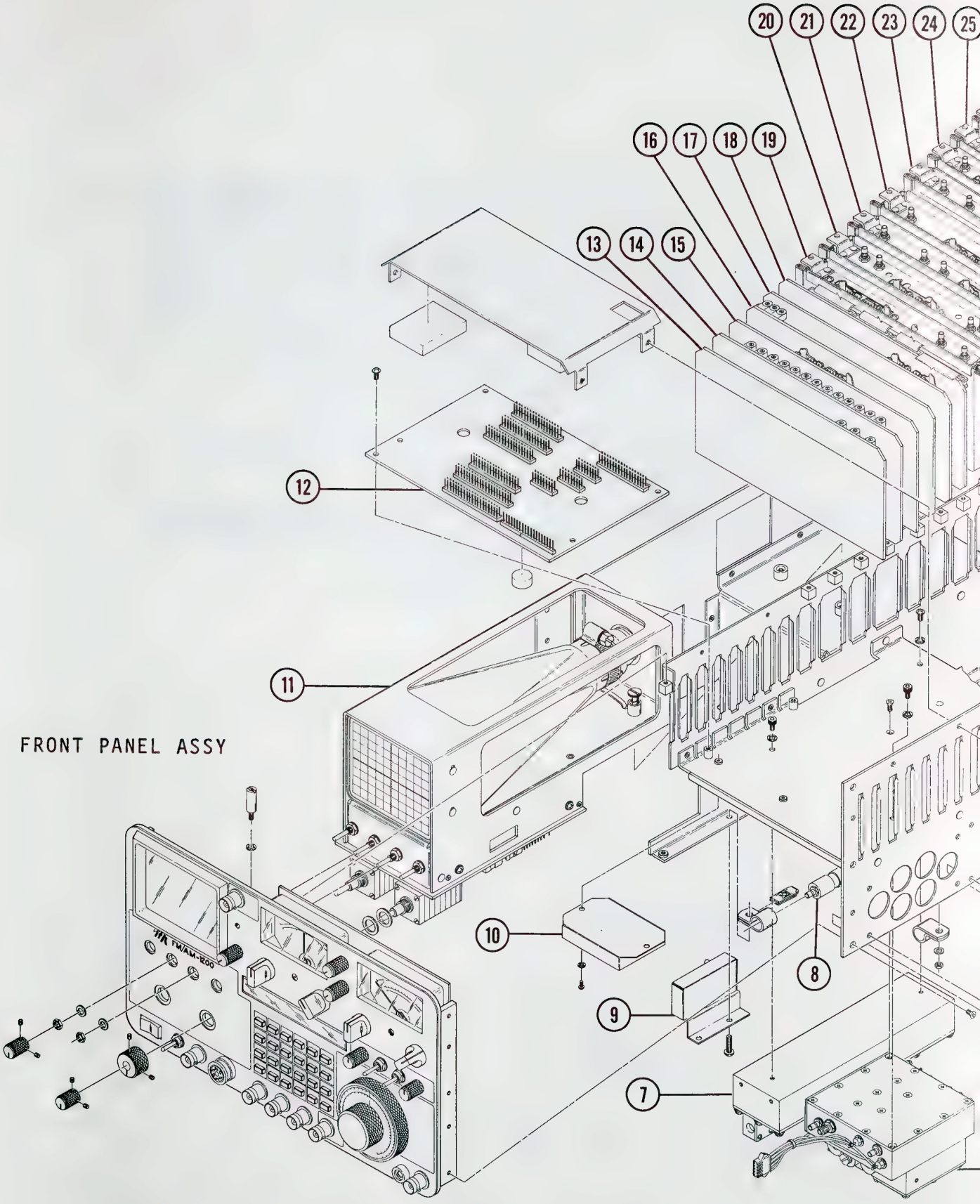
Output Amplifier Assembly
IF Module Assembly
Frequency Synthesizer Function
10.7 MHz Gen/Rec Assembly
Receive Audio PC Board
Generate Audio PC Board
Duplex Generator Assembly
Function Generator
Front Panel Monitoring Displays

6. Oscilloscope/Spectrum Analyzer

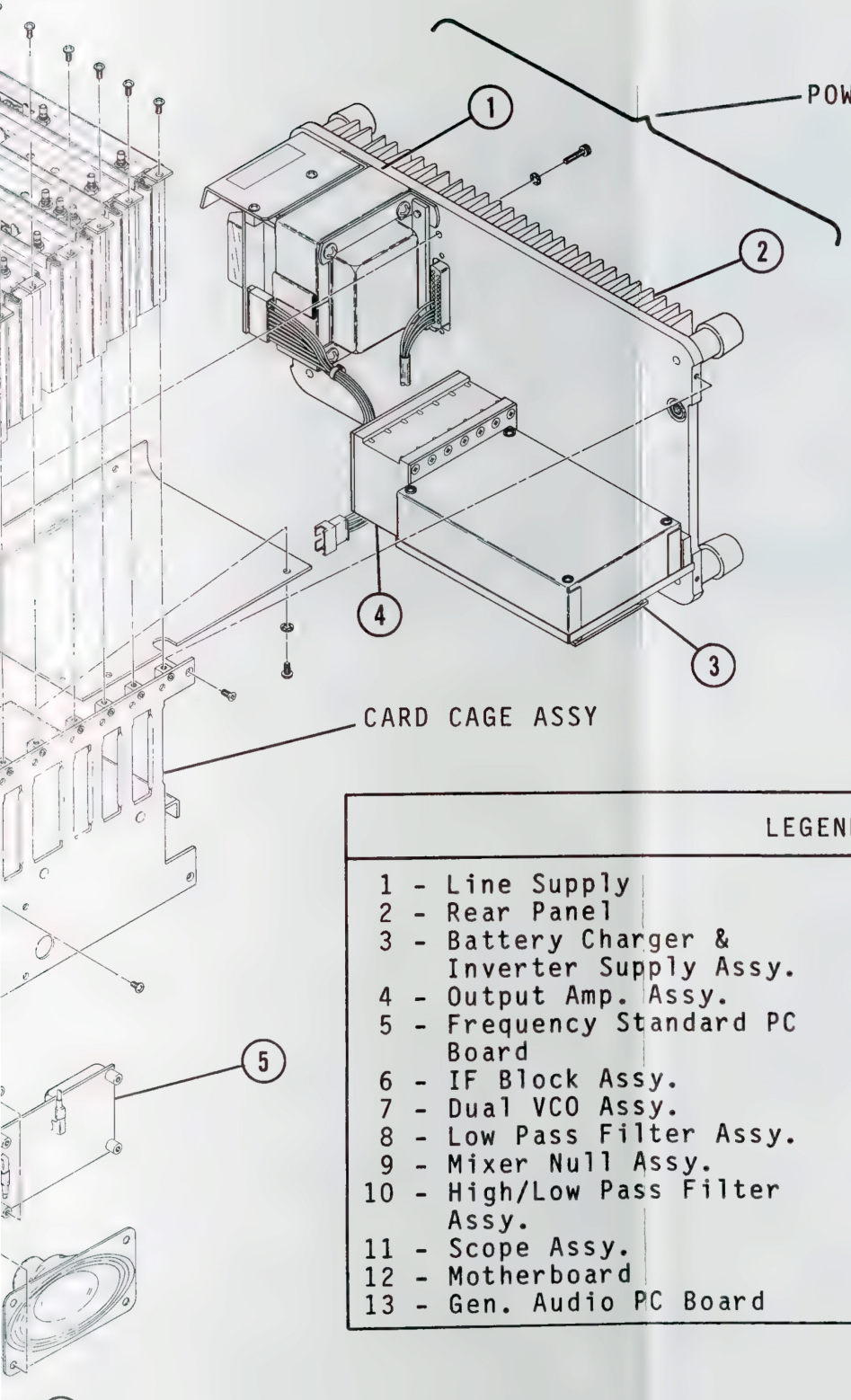
CRT Assembly
Scope Control PC Board
Scope Power Supply PC Board
Analyzer RF Assembly
Analyzer IF Assembly
Analyzer Log Amplifier Assembly

1-3 MECHANICAL DESCRIPTION

Figure 1-1 is an "exploded" composite view of the FM/AM-1200, identifying and locating its major assemblies. Front and rear panel controls, connectors and indicators are identified in Figure 1-2. This illustration foldout is to provide ready identification of references when performing testing or calibration of the FM/AM-1200.

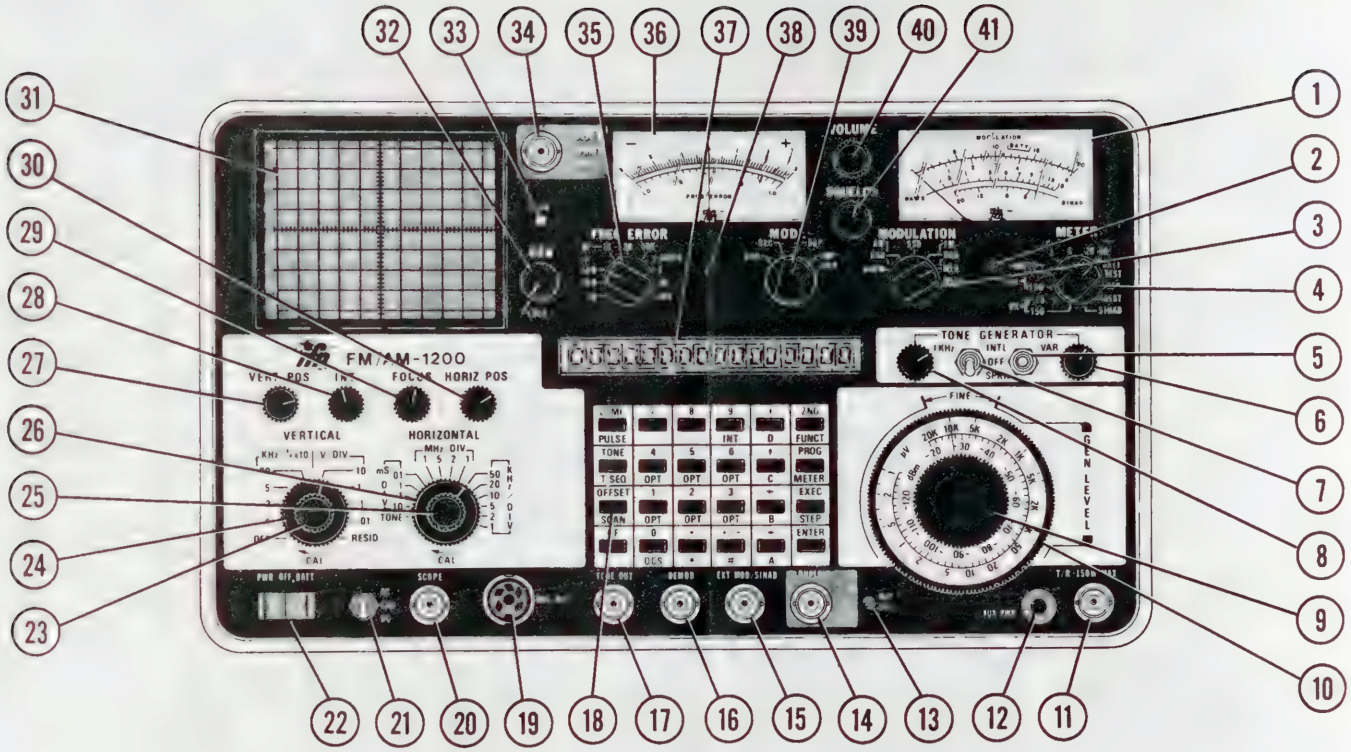


FRONT PANEL ASSY

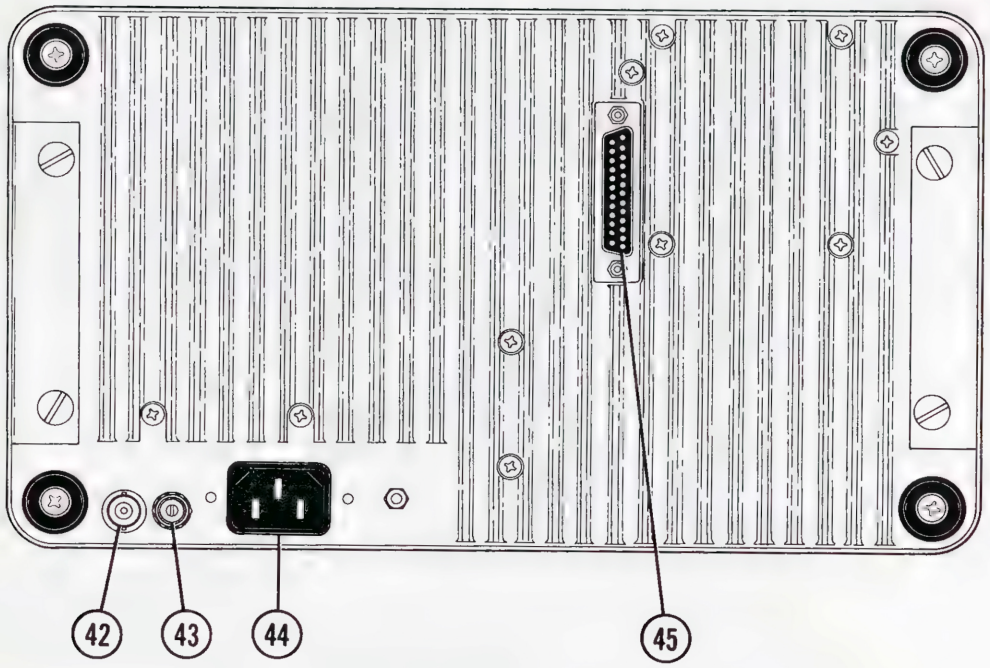


LEGEND	
1 - Line Supply	14 - Rec. Audio PC Board
2 - Rear Panel	15 - Tone Gen. PC Board
3 - Battery Charger & Inverter Supply Assy.	16 - DVM I/O PC Board
4 - Output Amp. Assy.	17 - CPU PC Board
5 - Frequency Standard PC Board	18 - Interface PC Board
6 - IF Block Assy.	19 - Low Loop Assy.
7 - Dual VCO Assy.	20 - High Loop Assy.
8 - Low Pass Filter Assy.	21 - Duplex Assy.
9 - Mixer Null Assy.	22 - Digital Assy.
10 - High/Low Pass Filter Assy.	23 - 10.7 MHz Gen/Rec Assy.
11 - Scope Assy.	24 - Analyzer RF Assy.
12 - Motherboard	25 - Analyzer IF Assy.
13 - Gen. Audio PC Board	26 - Analyzer Log Amp Assy.

Figure 1-1 FM/AM-1200 Composite (Module Identification)



1. MODULATION METER
2. Modulation Meter Zero Adjustment
3. MODULATION Select Control
4. Modulation METER Control
5. VAR Tone Selector Switch
6. VAR Tone Level Control
7. 1 kHz Tone Selector Switch
8. 1 kHz Tone Level Control
9. RF Level Attenuator Control
10. RF Level Attenuator Vernier Control
11. T/R Connector
12. AUX POWER Connector (Option 05 Gen. Amp only)
13. REF CAL Adjustment
14. DUPLEX Output Connector
15. EXT MOD/SINAD Connector
16. DEMOD Connector
17. TONE OUT Connector
18. Keyboard
19. MIC/ACC Connector
20. SCOPE Connector
21. AC/GND/DC Switch (Scope)
22. PWR/OFF/BATT Switch
23. Scope VERTICAL Attenuator Vernier Control
24. VERTICAL Attenuator Selector Control
25. Scope HORIZONTAL Sweep Vernier Control
26. HORIZONTAL Sweep Selector Control
27. VERT POS Control
28. INT Control
29. FOCUS Control
30. HORIZ POS Control
31. CRT Display
32. GEN/LOCK Control
33. LOCK Lamp
34. ANT Connector
35. FREQ ERROR Meter Range Selector Control
36. FREQ ERROR Meter
37. VFD (Vacuum Fluorescent Display)
38. FREQ ERROR Meter Zero Adjustment
39. MODE Selector Control
40. VOLUME Control
41. SQUELCH Control



42. RS-232 Connector
43. AC Power Input Connector
44. DC Power Input Connector
45. External Reference Connector

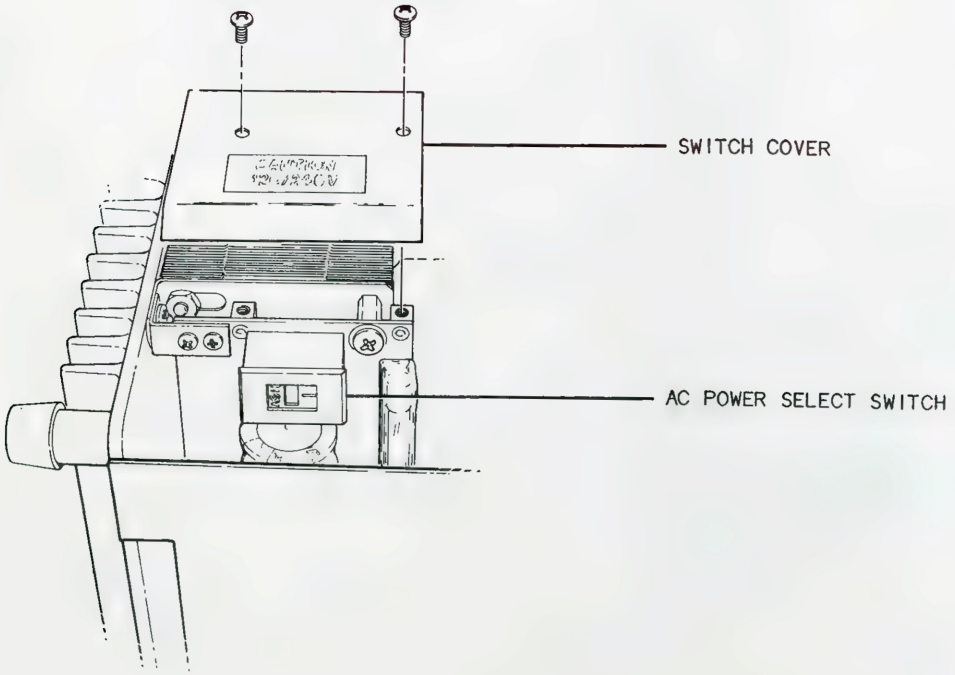


Figure 1-2 Description of Controls, Connectors & Indicators

SECTION 2 - THEORY OF OPERATION

2-1 GENERAL

This section contains three levels of Theory of Operation and is organized as follows:

1. SYSTEM THEORY OF OPERATION

   Paragraph 2-2 provides a simplified description of signal flow through the FM/AM-1200, for both receiver and signal generator operation. This description is based on the System Block Diagram shown in Figure 2-1. In addition, a brief overview of the oscilloscope and spectrum analyzer is covered within this paragraph.

2. FUNCTIONAL THEORY OF OPERATION

   Paragraph 2-3 provides a description of the major functional groupings in the FM/AM-1200. This description is based on the functional block diagrams for each grouping.

3. MODULE THEORY OF OPERATION

   Paragraph 2-4 provides detailed theory of operation for each module and/or assembly contained in the FM/AM-1200. All discussions are based on the accompanying block diagrams for each module.

2-2 SYSTEM THEORY OF OPERATION

The FM/AM-1200 is a processor controlled, digitally synthesized FM/AM/SSB receiver and generator, with an integral oscilloscope/spectrum analyzer. The receiver is a triple conversion superheterodyne receiver capable of receiving signals from 250 kHz to 999.9999 MHz. The signal generator is capable of producing modulated or unmodulated RF signals from 250 kHz to 999.9999 MHz. A function generator can produce six tone configurations (Ramp, Triangle, Square, Sine, DTMF and Pulse) to modulate the generator. A duplex generator can produce a signal up to ±49.99 MHz from the received frequency. The oscilloscope and spectrum analyzer utilize a common CRT. Bandwidth of the oscilloscope is DC to 1 MHz and the dynamic range of the spectrum analzyer is from -30 dBm to -100 dBm.

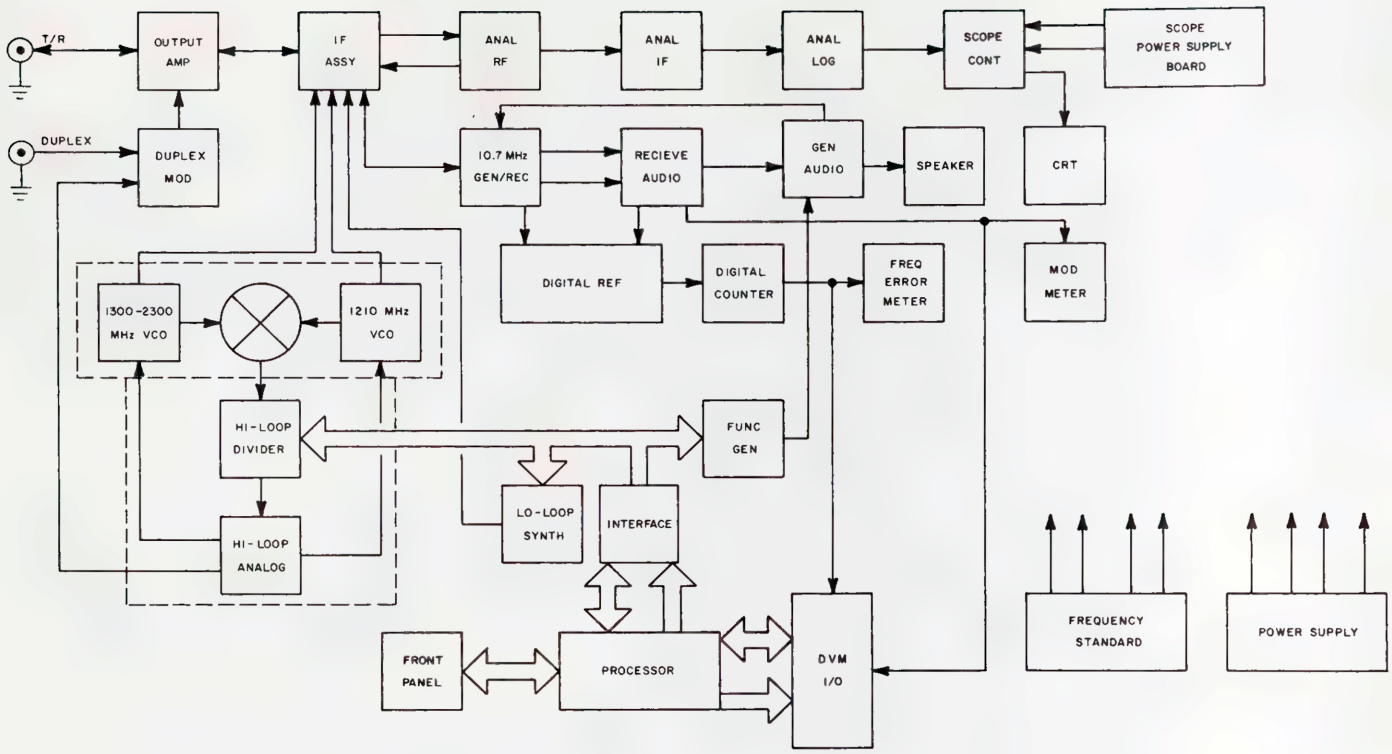


Figure 2-1 System Block Diagram

In the receive mode of operation, the input frequency is converted to 10.7 MHz in the IF Block Assy. The IF signal is filtered, amplified, then demodulated. This demodulated audio signal is then applied to the DEMOD Connector, to the Speaker through an audio amplifier, to the MODULATION Meter through a scaling circuit and to the frequency error counter for display on the FREQUENCY Error Meter.

In the generate mode of operation, the IF signal generator provides a frequency of 10.7 MHz, which can be either frequency or amplitude modulated. This signal is converted to the selected RF, amplified, then applied to the T/R Connector through a selectable and a fixed attenuator.

In the duplex mode, a separate signal generator produces an RF signal at a selected offset frequency of ±49.99 MHz. This offset frequency is then applied directly to the DUPLEX Connector and through a fixed attenuator to the T/R Connector.

The FM/AM-1200 function generator produces a ramp, triangle or square wave at frequencies between 10 Hz and 10 kHz, and a sinewave up to 30 kHz. The function generator also produces a composite DTMF and Pulse Signal. The selected signal (waveform) is applied to the TONE OUT Connector. This signal can also be used to modulate the 10.7 MHz IF or can be applied directly to the Speaker. An additional square wave is also generated, for use as a reference, during audio frequency error measurements. In addition, a 1 kHz sinewave is generated and applied to the TONE OUT Connector, and can be used to modulate the 10.7 MHz IF, or can be applied to the Speaker.

The FM/AM-1200 Oscilloscope is a single trace, 1 MHz unit which can be used to monitor demod audio, generate audio or external signals applied at the SCOPE Connector. The Spectrum Analyzer can be used to monitor generated or received signals. Received signal levels can be monitored from -30 dBm to -100 dBm.

2-3 FUNCTIONAL THEORY OF OPERATION

2-3-1 PROCESSOR OPERATION

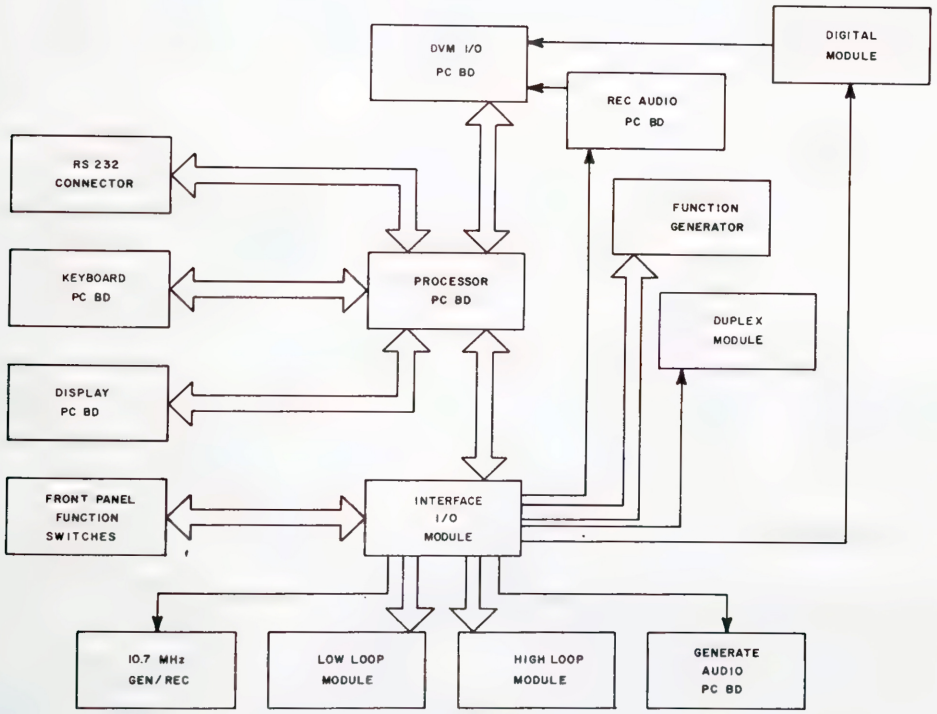


Figure 2-2 Processor Functional Block Diagram

The processor, through the Interface PC Board, transfers all data within the FM/AM-1200 over an internal data bus. It is the brain of the test set as it manipulates the data and allows the FM/AM-1200 to operate. It communicates directly with the Interface PC Board, Keyboard, VFD, DVM I/O PC Board and RS-232 Connector. The Interface PC Board communicates

directly with the High Loop Module, Low Loop Module, Function Generator PC Board, Duplex Module, Generate Audio PC Board, 10.7 MHz Gen/Rec Module, Digital Module, Receive Audio PC board, and front panel.

The processor contains two routines. The first routine is called the front panel routine which receives from the front panel, all data from the keyboard and control settings, processes this data and outputs the data to the hardware latches on the Interface PC Board to the other modules. The second routine of the processor is the RS-232 routine. The data flows exactly the same as in the first routine except all control inputs come through the RS-232 Connector.

2-3-2 RECEIVER SECTION OPERATION

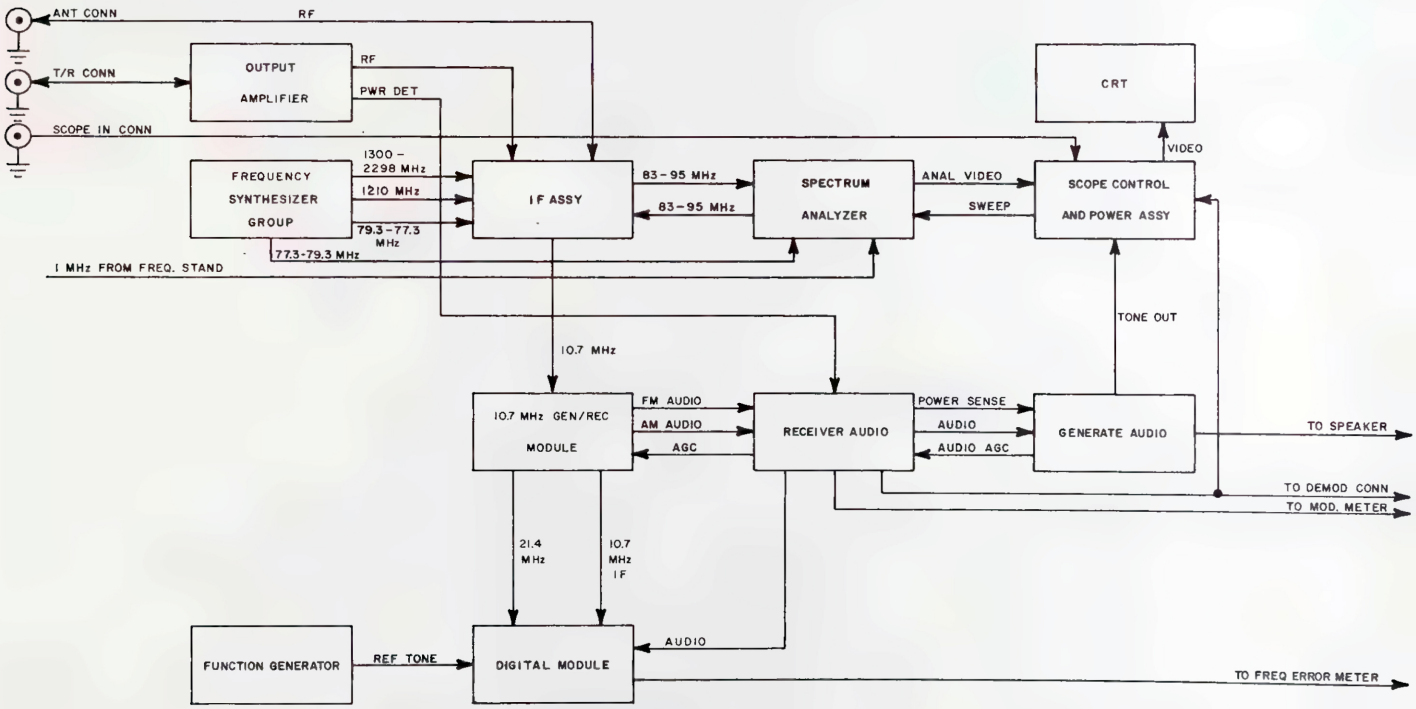


Figure 2-3 Receiver Functional Block Diagram

RF signals are received through either the ANT Connector or T/R Connector. Off-The-Air signals are received at the ANT Connector, whereas a transmitter under test is connected directly to the T/R Connector. The signal received at the T/R Connector is attenuated 80 dB and applied, in turn, to an antenna relay in the IF Block Assembly. Off-The-Air signals received at the ANT Connector are fed through a static protect circuit, RF gain stage and then to the antenna relay.

The signal received at the ANT connector is coupled through the antenna relay (which is normally energized) to the 1000 MHz Low Pass Filter in the IF Block Assembly. If a signal of 100 mW or greater is received at the T/R Connector, the relay is de-energized and the signal from the T/R Connector is coupled to the 1000 MHz low pass filter.

Whichever received signal source is selected, the received RF is converted twice in the IF Block Assy by two local oscillators in the dual VCO from the Frequency Synthesizer Group. This converted signal (83-95 MHz) is fed to the Spectrum Analyzer for display, and back to the IF module where it is down-converted to 10.7 MHz by a local oscillator signal from the Low Loop Synthesizer. The 10.7 MHz signal is fed to the 10.7 MHz Gen/Rec Module where it is bandpass filtered and demodulated. The 10.7 MHz Gen/Rec Module has an AM and an FM detector. The AM detector produces a DC level (AGC) proportional to the level of the 10.7 MHz IF input. When an AM signal is present, the demod audio signal will ride on this DC level. The FM detector produces a demodulated 10.7 MHz signal which is sent to the Digital module for frequency error measurements. When an FM signal is present, the FM detector also produces a demod audio signal. The demodulated audio signal out of the 10.7 MHz Gen/Rec Module is fed to the Receive Audio PC Board where it is amplified and audio bandpass filtered. The Receive Audio PC Board output is fed to the Generate Audio PC Board, front panel DEMOD Connector, Oscilloscope, front panel MODULATION Meter and Digital Module. The output from the Generate Audio PC Board is fed through an audio amplifier to the Speaker. The audio signal fed to the Digital Module is compared with a reference tone from the Function Generator to produce the audio error signal which is fed to the FREQUENCY ERROR Meter.

2-3-3 GENERATOR SECTION OPERATION

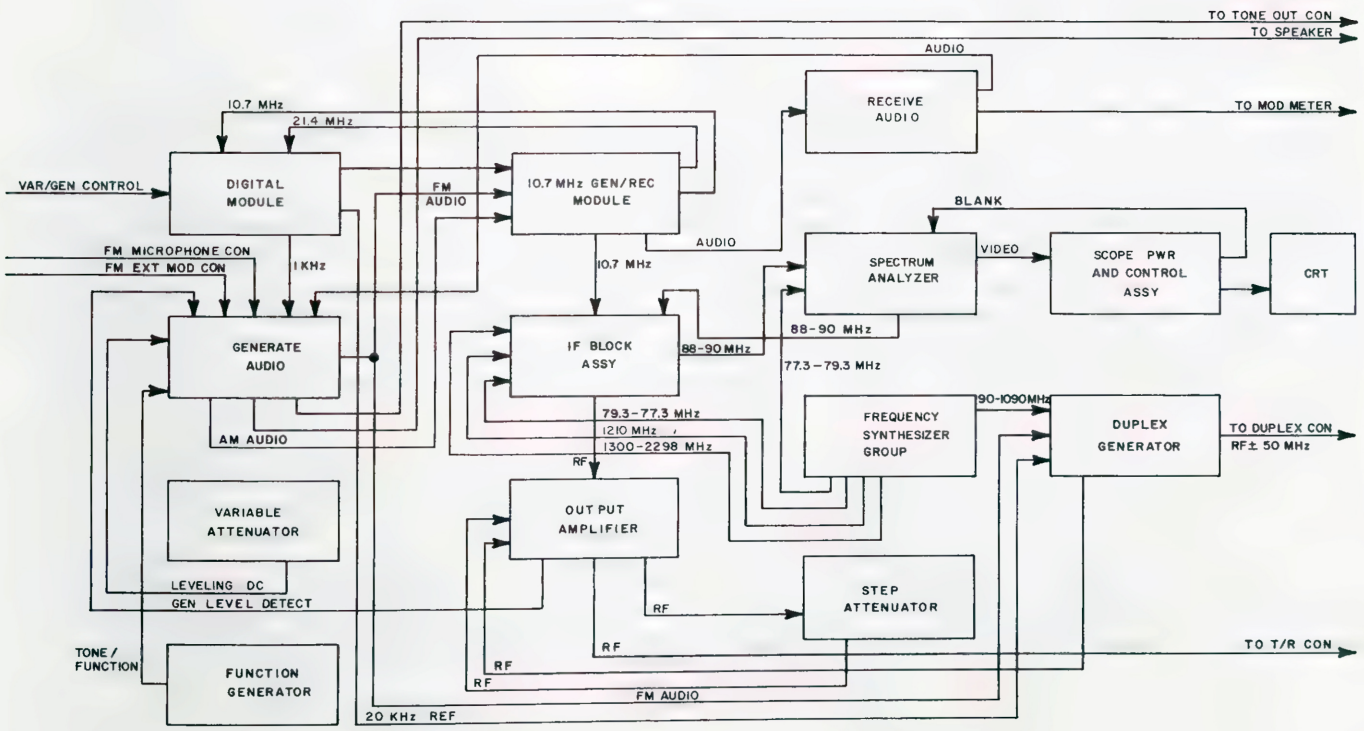


Figure 2-4 Generator Functional Block Diagram

In the generate mode, a 21.4 MHz VCO circuit in the 10.7 MHz Gen/Rec Module produces a 21.4 MHz signal. This signal is phase locked to the 10 MHz Frequency Standard by a phase lock loop in the Digital Module. The 21.4 MHz signal is divided by 2, to produce a 10.7 MHz IF, which passes through a leveler/modulator circuit for level control, then to the IF Block Assembly.

The 10.7 MHz IF is then mixed with the low loop synthesizer signal (77.3001 - 79.300 MHz) to produce an 88-90 MHz IF which is fed through an 89 MHz bandpass filter and amplified. At this point the 88-90 MHz IF is fed to the Analyzer RF Module for analyzer display, and to the second mixer in the IF Block Assembly. The second mixer mixes the 88-90 MHz IF with the 1210 MHz signal from the High Loop Synthesizer Module to produce a 1298-1300 MHz IF. This signal is amplified, filtered and fed to the third mixer. The third mixer mixes the 1298-1300 MHz IF with the 1300-2298 MHz signal from the High Loop Synthesizer Module to produce the selected RF signal. This signal is fed to a 1000 MHz low pass filter, then out of the IF Block Assembly to the Output Amplifier Assembly.

In the Output Amplifier, the RF signal is amplified, then its level is sampled to produce a level control signal to the leveler/modulator in the Generate Audio Module. Thus, the leveler/modulator circuit adjusts the level of the 21.4 MHz generator output sufficiently to vary 0-11 dB at the Output Amplifier. The RF signal then goes to a 10 dB step attenuator for operator generator level selection, then back to the Output Amplifier, where it is attenuated an additional 20 dB. The signal is then routed to the T/R Jack and to the Unit Under Test.

To amplitude modulate the carrier, internal signals from the Digital Module (1 kHz sinewave) and Variable Tone Generator, and external signals from the MIC/ACC and EXT MOD Jacks are combined in the leveler/modulator circuit of the Generate Audio Module. For frequency modulation, the output from the generate audio PC board varies the 21.4 MHz generator frequency; for amplitude modulation, the combined audio signal is fed to the fine attenuator. The output of the fine attenuator is summed with the control voltage from the output amplifier on the generate audio PC board. This signal is fed to the 10.7 MHz GEN/REC Module where it controls the RF output level and AM modulates the 10.7 MHz signal.

The Duplex Generator receives a 20 kHz reference frequency from the Digital Module and a 90-1088 MHz signal representing the selected RF from the High Loop Module in the Frequency Synthesizer. According to the frequency offset selected, the generator frequency is up to 49.99 MHz above or below the selected RF. One output is through the DUPLEX Jack on the Front Panel at -60 dBm. A second output is to the Output Amplifier, where it is attenuated 20 dB, then out through the T/R Jack.

2-3-4 FREQUENCY SYNTHESIS OPERATION

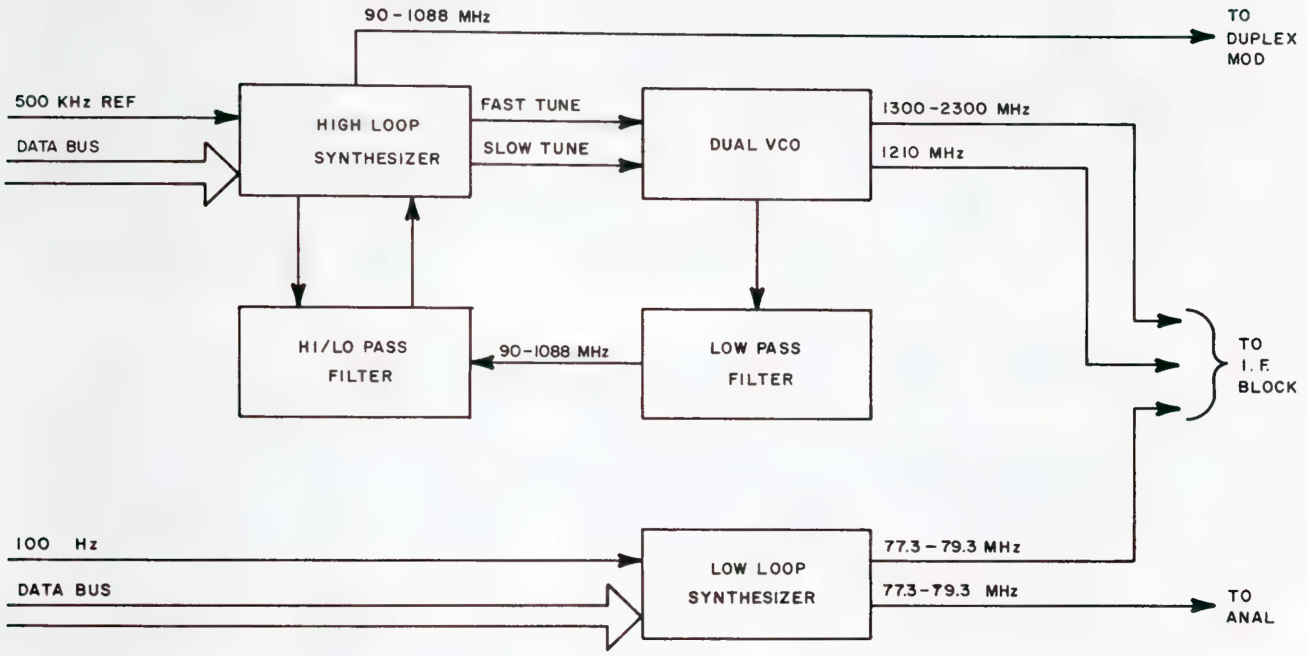


Figure 2-5 Frequency Synthesis Functional Block Diagram

The Frequency Synthesis Group consists of the High Loop Synthesizer, Low Loop Synthesizer, Low Pass Filter and Hi/Low Pass Filter. The Low Loop Synthesizer generates a 77.3-79.3 MHz signal that is selectable in 100 Hz steps. This signal is fed to both the IF Block Assy and Analyzer RF Module. The High Loop Synthesizer generates two DC voltages which control two separate oscillators in the Dual VCO Module. One oscillator operates at 1300-2300 MHz, while the other operates at 1210 MHz. Both the 1210 MHz and 1300-2300 MHz signals are fed to the IF Block Assy in addition to being mixed within the module to produce a 90-1088 MHz signal which is fed, through the Low Pass and Hi/Low Filters to the High Loop Module where it is divided down and compared with a 500 kHz reference signal received from the Frequency Standard PC Board. The 90-1090 MHz signal is also sent from the High Loop Synthesizer Module to the Duplex Module.

2-3-5 REFERENCE FREQUENCY OPERATION

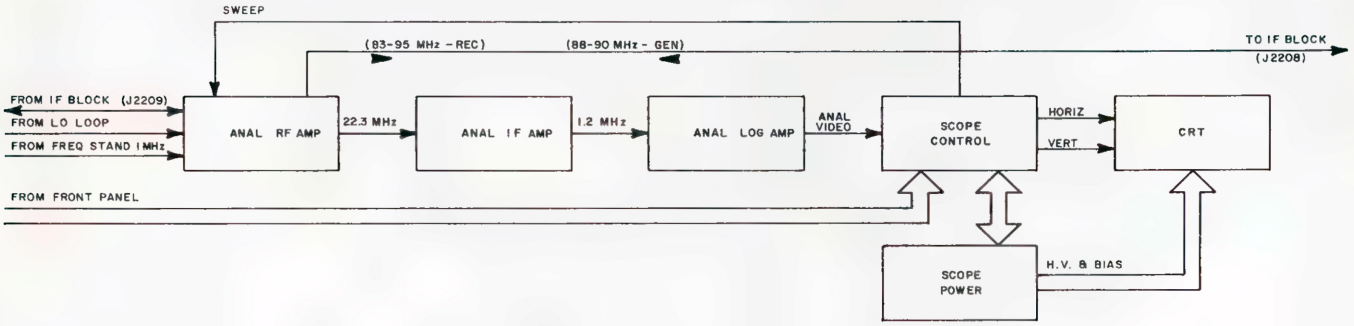


Figure 2-6 Reference Frequency Functional Block Diagram

The FM/AM-1200 uses 10 MHz as the primary standard frequency. A TCXO (Temperature Compensated Crystal Oscillator) or an optional oven oscillator normally produces this frequency. An external 10 MHz standard can also be used in place of the TCXO. The Frequency Standard divides the 10 MHz to 1 MHz which is sent to the Digital Module and Analyzer RF Module, and to 500 kHz which is fed to the High Loop Synthesizer Module. The Digital Module further divides the 1 MHz signal to 20 kHz which is fed to the Duplex Module, to 1 kHz sine wave which is sent to the Generate Audio PC Board and to 100 Hz which is fed to the Low Loop Synthesizer Module.

2-3-6 OSCILLOSCOPE/SPECTRUM ANALYZER OPERATION

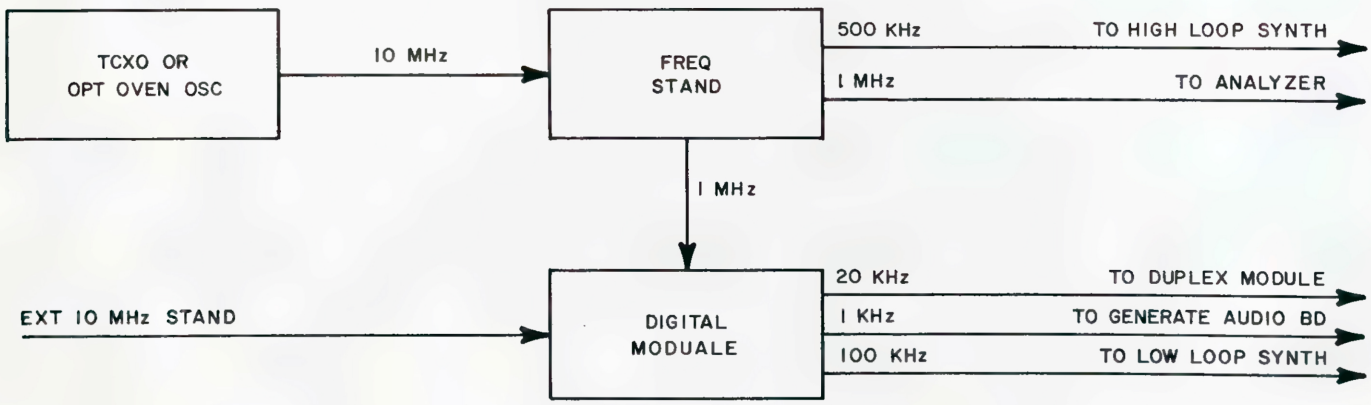


Figure 2-7 Oscilloscope/Spectrum Analyzer Functional Block Diagram

During analyzer operation, an 83-95 MHz signal is sent from the IF Block Assy to the Analyzer RF Module where it is mixed with a sweep oscillator, centered at 111.3 MHz, producing a 22.3 MHz signal which is fed to the Analyzer IF Module. The 22.3 MHz signal is mixed with a 33 MHz signal in the Analyzer IF Module, producing a 10.7 MHz signal. This signal is then filtered and mixed with a 9.5 MHz signal, producing a 1.2 MHz signal which is fed to the Analyzer Log Amp Module. In the Analyzer Log Amp Module, the amplitude of the 1.2 MHz signal is converted from a logarithmic value to a linear value and fed to the Scope Control PC Board for presentation on the Scope (CRT). The Scope Power PC Board supplies all voltages necessary to bias the CRT. It also supplies the voltages for horizontal and vertical deflection to the Scope Control PC Board.

The Scope Control PC Board receives signals from the Front Panel (Tones, Demod, Residual Distortion and SCOPE Connector). The signal selected for display is attenuated, sent to the vertical deflection amplifier and to a triggering circuit. Sweep speed is selected and sent to the horizontal deflection amplifier. The horizontal and vertical deflection signals are sent from the Scope Control PC Board to the CRT for display. The sweep signal is sent to the Analyzer RF Module to control the sweep oscillator.

2-4 DETAILED THEORY OF OPERATION

The theory of operation for each module contained within the FM/AM-1200 is discussed, in detail, in the following paragraphs. In addition to the detailed block diagrams, which are included with each topic, reference should be made to the appppropriate schematic or interconnect drawing contained in Section 6.

2-4-1 POWER SUPPLY MODULE

The Power Supply System consists of three major components:

Line Supply Assembly - which is an AC to DC converter containing a power transformer, voltage select switch, bridge rectifier and filter.

Inverter Supply PC Board - which is a DC to DC converter utilizing a duty cycle regulator, transformer and rectifier and filter circuits which furnish the various voltages utilized throughout the test set.

Battery Charger PC Board - which is mounted on the Power Supply Assy, contains the battery charger circuit and selects the power source for the Inverter Supply PC board.

When the optional oven oscillator frequency standard is installed, an oven supply voltage regulator is also included on the Battery Charger PC Board.

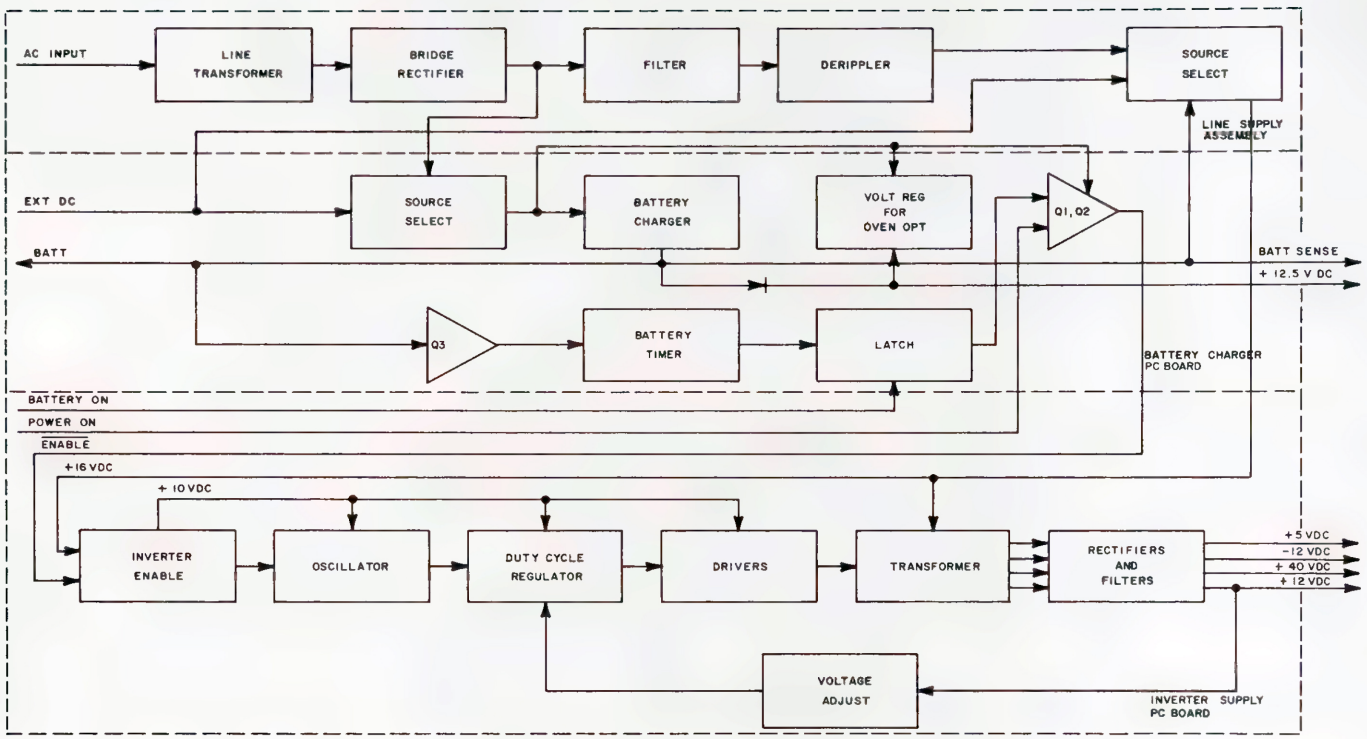


Figure 2-8 Power Supply Module Block Diagram

A. LINE SUPPLY ASSY

The AC Power Input Connector on the rear panel is connected to the Line Supply Assy through J1701. Power is supplied to T1701 through F1701 and SW1701. T1701 has two primary windings which are connected in parallel when 115 VAC is selected by SW1701, or in series if 230 VAC is selected. The secondary winding of T1701 is connected to full wave rectifier, BR1701, which is mounted on the rear panel heat sink. C1701 and C1702 filter and deripple the +16 VDC (nominal). Unregulated voltage from BR1701 is applied to the Battery Charger PC Board for charging the battery, operating the inverter on/off switching, and provides oven supply voltage for the optional oven oscillator.

Regulated voltage from Q4601 is applied through the Battery Charger PC Board to the Inverter Supply PC Board.

B. BATTERY CHARGER PC BOARD

External DC power, filtered +16 VDC from the Line Supply Assy and the battery are all independently applied to the Battery Charger PC Board through J1601. All three sources are compared by diodes CR1601, CR1602 and CR1603 respectively, and the highest voltage source (Ext. DC or AC) is applied through fuse F1601 to the Inverter Supply PC Board. The external DC and unfiltered +16 VDC from the Line Supply Assy are applied through CR1605 and CR1606 to the battery charger circuit, inverter enable circuit and, if installed, the optional oven oscillator voltage regulator.

The battery charger circuit consists of adjustable regulator U1601, R1601 thru R1604 and C1601. R1602, R1603 and trimpot R1604 form a voltage divider to adjust the output voltage to 14.4 VDC and R1601 provides a minimum load to regulator U1601. Anytime AC or DC power in excess of the battery level is applied to the test set, the battery charger circuit will charge the battery. The position of the PWR/OFF/BATT Switch does not affect the charging circuit.

Q1601, Q1602, Q1604 and associated components make up the inverter enable circuit. When AC or DC power is applied, and the PWR/OFF/BATT Switch is in the OFF position, Q1601 does not conduct. However, with the PWR/OFF/BATT Switch in the PWR position, Q1601 will conduct, in turn Q1602 is turned on, pulling down on the inverter enable line, causing Q1501 on the Inverter Supply PC Board to conduct. If external AC power is interrupted, diodes CR1602 and CR1603 switch the inverter supply to the battery, while capacitors C1701 and C1702 in the Line Supply Assy keep Q1601 and Q1602 turned on for approximately 10 seconds while they discharge. As the voltage drops, the base to emitter voltage difference on Q1601 decreases until it is shut off. This, in turn, shuts off Q1604 driving the voltage to the base of Q1601 higher, preventing oscillation.

The battery enable circuit consists of flip-flop U1602B and related components. When the PWR/OFF/BATT Switch is depressed in the batt position, C1604 is allowed to charge through R1610, clocking U1602B to high Q, which turns on Q1602 and, subsequently, the Inverter Supply PC Board. Depressing the PWR/OFF/BATT Switch a second time clocks U1602B to low Q condition. If U1602B is not clocked the second time, approximately ten minutes later, a timer circuit will reset U1602B to a low Q condition.

Programmable timer U1603 starts counting as soon as the Inverter Supply PC Board supplies +12 VDC to the Battery Charger PC Board, regardless of the selected power source. A terminal count is set by highs on pins 9 through 12 and the on-chip oscillator frequency is established by R1617, R1618

and C1607 to allow approximately 10 minutes of battery operation. At this time, U1603 provides a high output to reset U1602B to a low Q condition to terminate battery operation.

A low battery cutoff circuit stops battery operation if the battery voltage drops below approximately +11.4 VDC. +12 VDC is applied to the emitter of transistor Q1603 while the battery voltage is applied to its base. When the battery voltage drops to approximately 11.4 VDC, Q1603 turns on, applying +12 VDC to the SET pin of U1603. This sets the timer to terminal count, providing a high output to reset U1602B. Q of U1602B then goes low, terminating battery operation.

C. INVERTER SUPPLY PC BOARD

The Inverter supply PC Board contains a duty cycle regulator, transformer and rectifier circuits which produce the regulated +12VDC, +5VDC, +40VDC and -12VDC which are distributed throughout the test set. The inverter supply voltage from the Battery Charger PC Board is +12VDC to +30VDC, depending upon the source.

When the test set is turned on, the low enable line pulls down on the bases of Q1501 and Q1505. Q1501 conducts, allowing +10VDC, set by Zener diode CR1503, to supply power to op amps U1501, U1502 and U1503 and through a voltage divider using R1503 and R1504, to the non-inverting input of U1501. Simultaneously, Q1505 is turned off, allowing U1501 to produce a sawtooth output at approximately 45 KHz which is applied to the non-inverting input of U1502.

Zener diode CR1505 applies a 6.9 VDC reference to the inverting input of U1503 which is configured as an integrator. A sample voltage from the +12 VDC secondary winding of T1501, after being rectified by CR1508 and C1510, passes through a voltage divider, consisting of R1510, R1511 and trimpot R3901 for calibration and is applied to the non-inverting input of U1503. As power is applied to the primary winding of T1501, C1510 becomes charged through CR1508. As the voltage at C1510 rises, the voltage at pin 3 of U1503 rises proportionately, increasing the output voltage at pin 6 which is the reference level for U1502.

U1502 compares the oscillator output level with the reference level from U1503, and produces a pulsed output whose duty cycle decreases as the reference level increases. R1514 sets a minimum reference level to maintain a maximum duty cycle of 50%. The high output from U1502 turns on Q1502, applying voltage to the gates of Q1504 and Q1506. Q1504 and Q1506 conduct, pulling current through the primary winding of T1. When U1502 output goes low, Q1502 is turned off, blocking voltage to Q1504 and Q1506, and Q1503 is turned on. This then turns off Q1504 and Q1506. The result of this action is to build, then collapse the magnetic field from the primary winding of T1501 proportionately to the duty cycle of U1502.

The power induced by the primary winding of T1501 into the secondary windings is proportional to the amount the magnetic field has developed during the duty cycle of U1502. Because the test set loads on the +5 VDC, +40 VDC and -12 VDC supplies are constant. These three track the +12 VDC supply. As the load on the +12 VDC supply varies, as with the use of the Oscilloscope or Spectrum Analyzer, integrator U1503 detects the effect on the +12 VDC supply line and raises or lowers the duty cycle reference level at U1502 accordingly. Increasing the load on the +12 VDC supply increases the duty cycle, which increases the transfer of power from the primary winding of T1501 to the secondary windings.

The AC voltages from the secondary windings are half-wave rectified by individual diodes. The +40 VDC supply is RC filtered; the other supplies are LC filtered.

2-4-2 PROCESSOR PC BOARD

The Processor PC Board contains a microcontroller (CPU) U101, system ROM U107, option ROM U108, RAM U109, latch U103, decoder U105, converters U110 and U111, buffers U102, U104 and U106, and associated components.

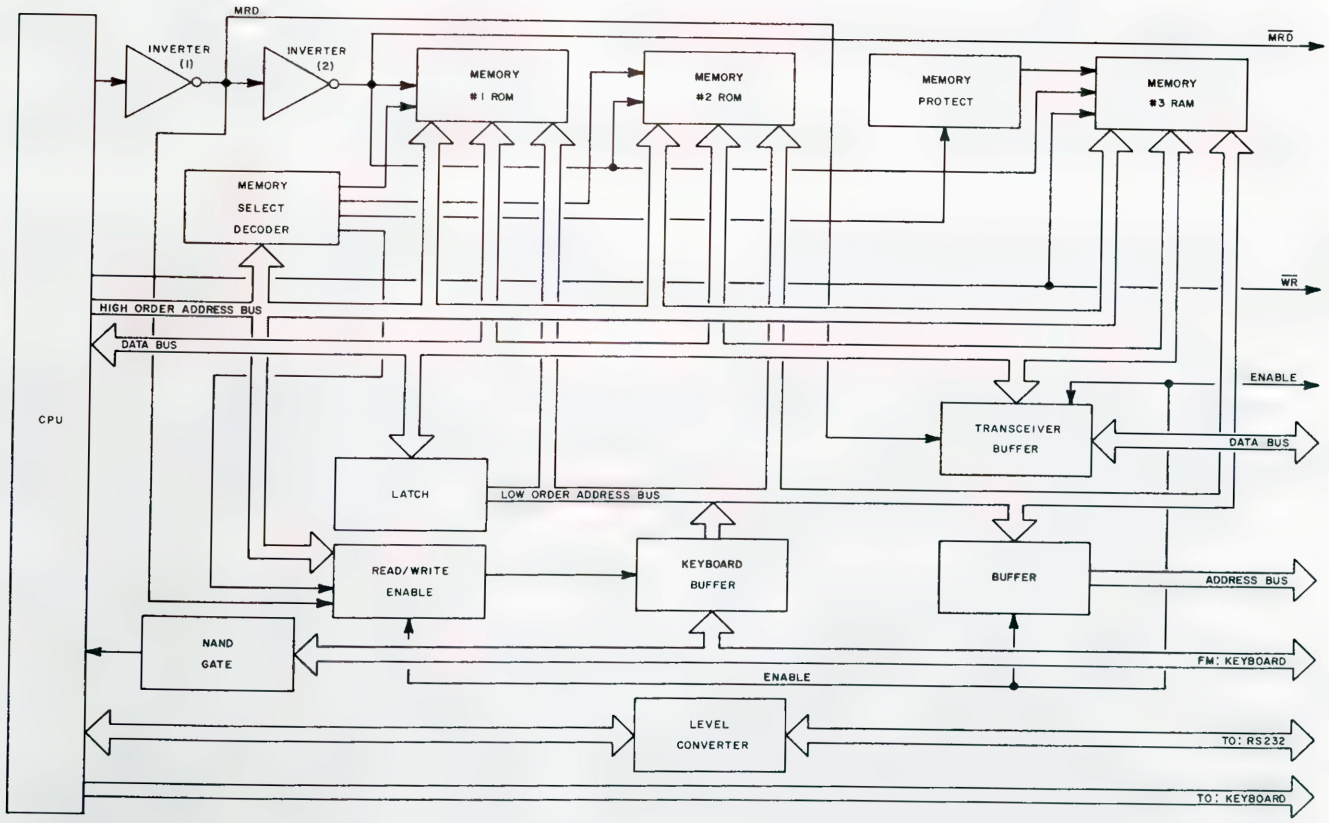


Figure 2-9 Processor PC Board Block Diagram

The CPU has four 8-bit parallel ports, of which three are used to address the three buses in the FM/AM-1200. Port 0 functions as a data bus and the low order address bus which is buffered through latch U103. The low order address bus is for addressing the peripheral components. Port 2 is the high order address bus and is used for addressing memory. Bits 0 thru 3 of Port 1 are devoted to the Keyboard PC Board, bits 4 and 5 of Port 1 provide data and clock signals to the Display PC Board and bits 6 and 7 of Port 1 provide the RTS (Ready-To-Send) and CTS (Clear-To-Send) control signals to the RS-232 Connector. Port 3, the fourth port, serves as special function port and is used as follows:

BIT NO.	FUNCTION
0	RXD (Serial Input Port)
1	TXD (Serial Output Port)
2	$\overline{\text{INT0}}$ (External Interrupt)
3	$\overline{\text{INT1}}$ (External Interrupt)
4	T0 (Timer/Counter 0 External Input)
5	T1 (Timer/Counter 1 External Input)
6	$\overline{\text{WR}}$ (External Data Memory Writer Strobe)
7	$\overline{\text{RD}}$ (External Data Memory Read Strobe)

Table 2-1 Port 3 Pin-Out Table

Y101 is an 11.059 MHz crystal for the on-chip oscillator in U101. U110 converts the TTL data from U101 to +12 VDC and -12 VDC required by the RS-232. U111 converts the +12 VDC and -12 VDC from the RS-232 to TTL data required by the CPU, U101. U103 is the address latch for the low eight bits of the address line and U105 is a decoder/demultiplexer used to address the peripheral components.

ROM U107 contains all the main operating functions such as RF controls, tone control and tone sequences. If option ROM U108 is installed, when addressed, a new set of vectors is set up and any options contained in ROM can then be addressed through the keyboard.

The memory protect circuit, consisting of Q101 thru Q104, and associated components is a voltage comparator which detects when voltage is removed from the test set. A backup +3V Lithium Battery (BT101), which is part of the memory protect circuit, is placed in line with RAM U109, so when power is removed, the memory contents in RAM will be retained. This is accomplished by placing +3 VDC on pin 28 of U109.

In the keyboard circuit, bits 0 thru 3 of Port 1 from U101 are the row lines for the keyboard and are driven low by the CPU. The column lines for the keyboard (pins 1, 2, 3, 5, 7, 9 of J103) are held high by +5 VDC through RN101 and monitored by NAND/AND gate U114. When a button on the keyboard is depressed, one of the column lines will be driven low, detected by U114, causing it to change states, generating an interrupt in the CPU. During this interrupt routine, the row lines are driven low one at a time. As each row line is driven low, the column lines are read by the CPU through buffer U104. After all four row lines have been strobed and all column lines read, the CPU determines which button was depressed and enters a routine for that button. If more than one button is depressed, no action is taken by the CPU.

2-4-3 INTERFACE PC BOARD

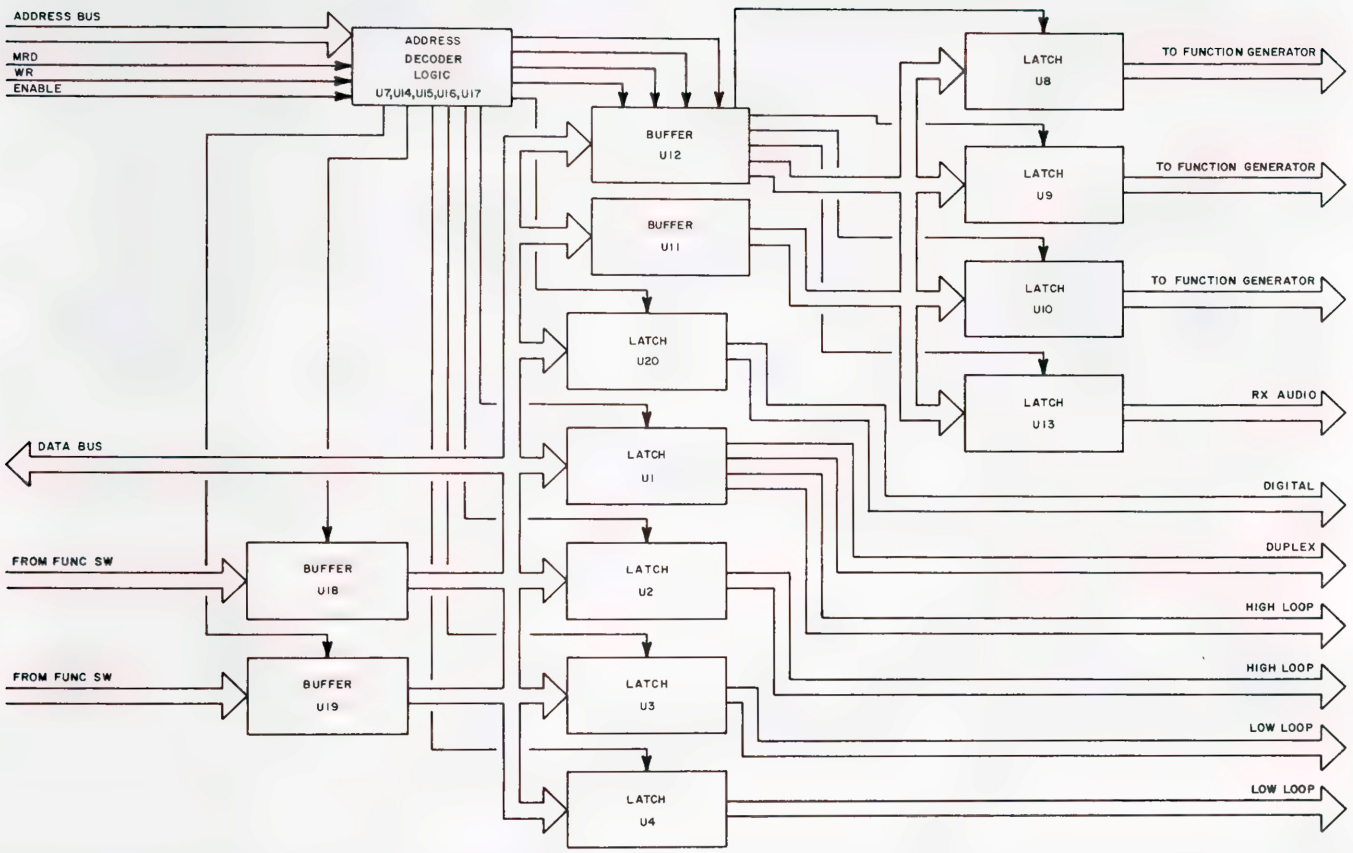


Figure 2-10 Interface PC Board Block Diagram

The Interface PC Board latches all data from the Processor PC Board to the following: Function Generator, High Loop Assy, Low Loop Assy, Receive Audio PC Board, Digital Module, and the Duplex Module. Data from the Function Switch PC Board is buffered on the Interface PC Board before being sent to the processor.

The address decoder (U1007, U1014, U1015, U1016 and U1017) decodes the 8-bit address bus and the 3-control lines ($\overline{MRD}$, $\overline{WR}$, Enable) to set the latches or read the buffers.

2-4-4 DVM I/O PC BOARD

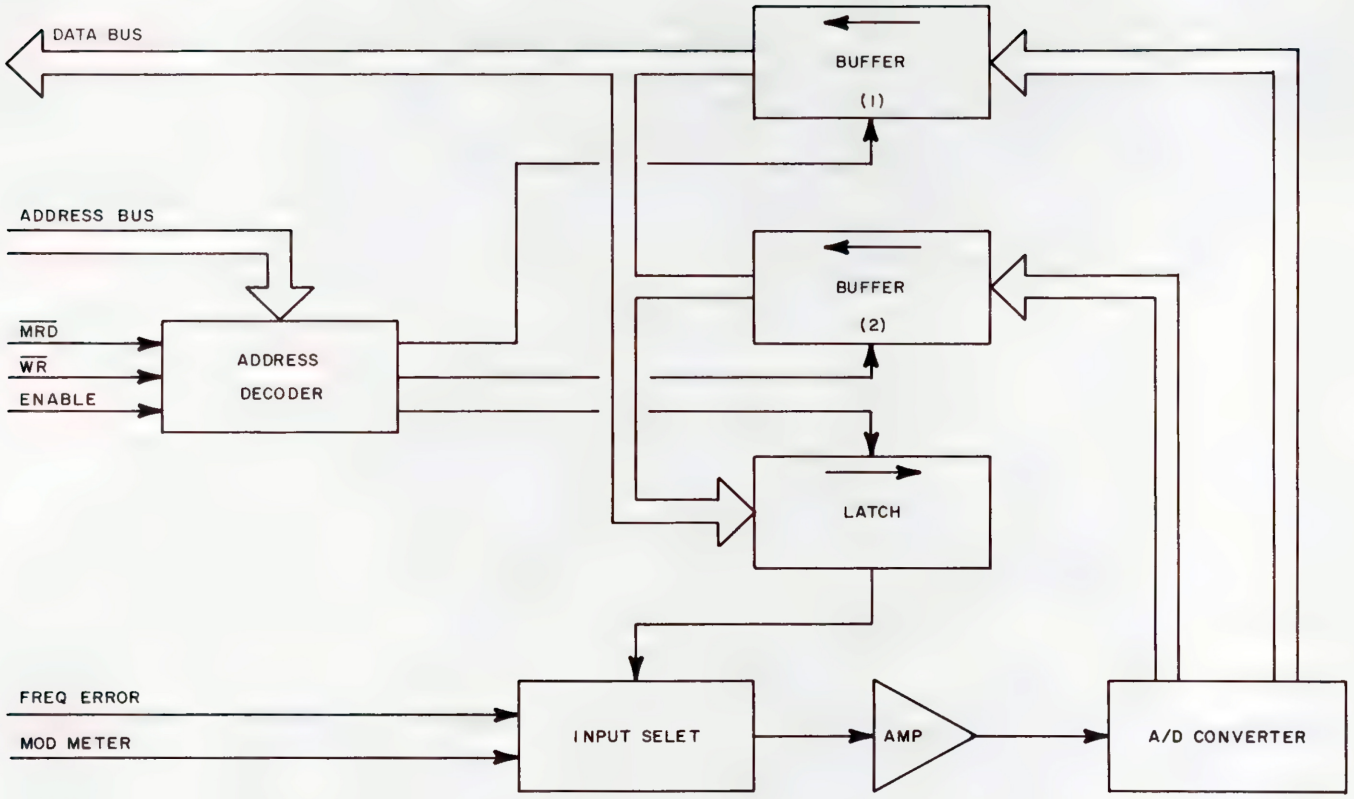


Figure 2-11 DVM I/O PC Board Block Diagram

The DVM I/O PC Board is basically an analog to digital converter. Signals received from the Digital Module and the Receive Audio PC Board are converted to digital form, for presentation on the Vacuum Fluorescent Display.

Frequency error and modulation monitor signals are routed to the input select chip U3009. Signal selection is made when the address decoder (U3003, U3004, U3005, and U3006) clocks the DØ data bit through Latch 1 U3008. If DØ is low, FREQ Error is switched to op amp U3012. When DØ is high, mod monitor is switched to the amp. From the op amp, the selected signal is sent to A/D converter (U3010) where it is digitized. This digital signal is then buffered by U3002 and U3007 and sent to the Processor PC Board via the data bus.

2-4-5 FREQUENCY STANDARD PC BOARD

The Frequency Standard uses a voltage controlled, Temperature Compensated Crystal Oscillator (TCXO) to furnish a constant 10 MHz reference frequency. When desired, an external 10 MHz reference signal can be used by connecting the signal source to the External Reference Connector on the rear panel of the test set. A bi-quinary ripple counter divides the 10 MHz signal to a 500 kHz signal which is fed to the High Loop Module, and to a 1 MHz signal which is fed to both the Digital Module and Spectrum Analyzer RF Module.

A level detect circuit determines when an external 10 MHz reference signal of sufficient amplitude is present on the External Reference Connector and responds by deactivating the TCXO and couples the external 10 MHz reference signal to the frequency divider.

The internal 10 MHz reference signal produced by the TCXO is also fed back to the rear panel External Reference Connector, which can be used during calibration.

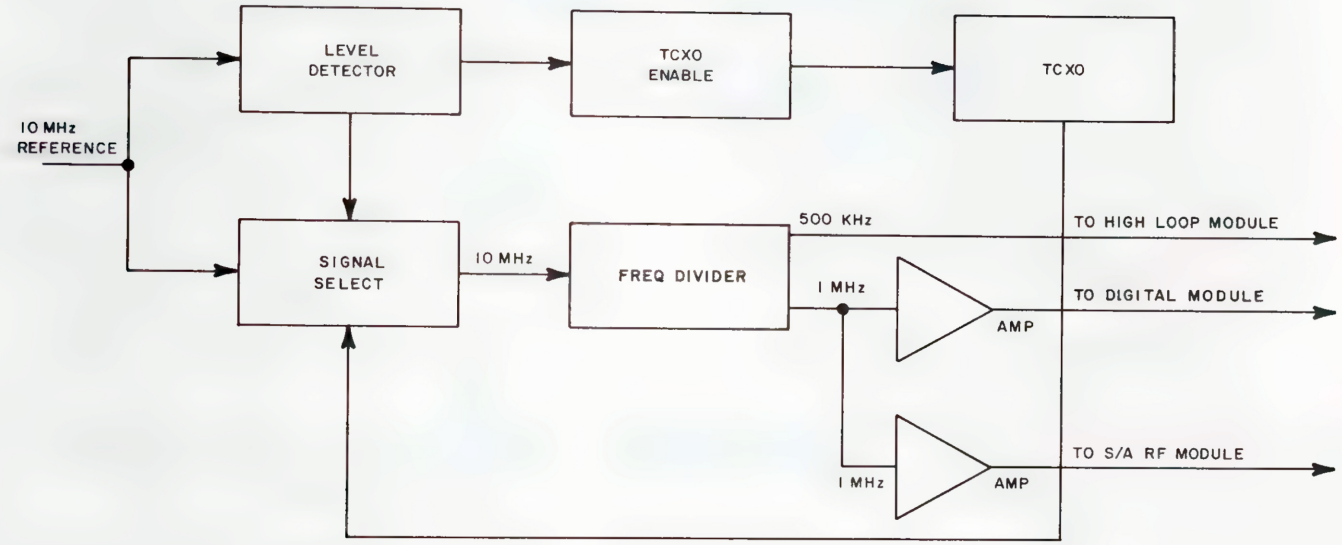


Figure 2-12 Frequency Standard PC Board Block Diagram

When an external 10 MHz reference signal exceeding 5 V p-p is applied through the External Reference Connector to NAND gate U2802, a level detector, consisting of op amp U2801 and associated components, produces a constant high, turning off Q2801 and interrupting power to the TCXO. The high output of U2801 is also fed to U2802, passing the external 10 MHz reference signal to the frequency divider circuit.

The internal 10 MHz reference signal from the TCXO is applied to pin 9 of NAND gate U2802. The gated output from U2802, pin 6 is fed to U2803 and through R2807 to the External Reference Connector.

The level detector in the signal select circuit controls the base voltage to transistor Q2801, which, in turn, controls the +12 VDC to the TCXO. R3501 on the front panel allows fine adjustment of the operating frequency to calibrate the TCXO. The TCXO course adjustment is within the TCXO Assy mounted on the Frequency Standard PC Board.

The frequency divider circuit consists of dual counter U2803, two buffer transistors, Q2802 and Q2803, and associated components. The 10 MHz input is divded by 10 in the first counter applied to the base of both transistors. Q2802 supplies a 1 MHz reference frequency to the Digital Module through P402 and Q2803 supplies 1 MHz to the Spectrum Analyzer through P404. The output of the first counter is further divided to 500 kHz and sent to the High Loop Module through P4001.

2-4-6 DIGITAL MODULE

The Digital Module contains 2 PCBs, the Digital Reference PC Board and the Digital Counter PC Board. The Digital Reference PC Board receives a 1 MHz signal from the Frequency Standard and divides it down for use throughout the FM/AM-1200.

SIGNAL	DESTINATION	USE
20 kHz	Duplex Module	REF Freq
10 kHz	Digital Counter PCB	Time Base*
1 kHz	Digital Counter PCB	Time Base*
1 kHz	Digital REF	REF Freq for 21.4 MHz OSC
1 kHz Sine	Front Panel	Fixed Tone
100 Hz	Low Loop Assy	REF Freq
100 Hz	Digital Counter	Time Base*
10 Hz	Digital Counter	Time Base*

* These signals are used in the Digital Counter PC Board for FREQ Error Measurements.

The Digital Reference PC Board also contains a 1 kHz sine wave filter, phase lock loop for the 21.4 MHz oscillator on the 10.7 MHz Gen/Rec Module, and tone multipliers for audio error measurements.

The Digital Counter PC Board contains all logic and counters for FREQ Error Measurements.

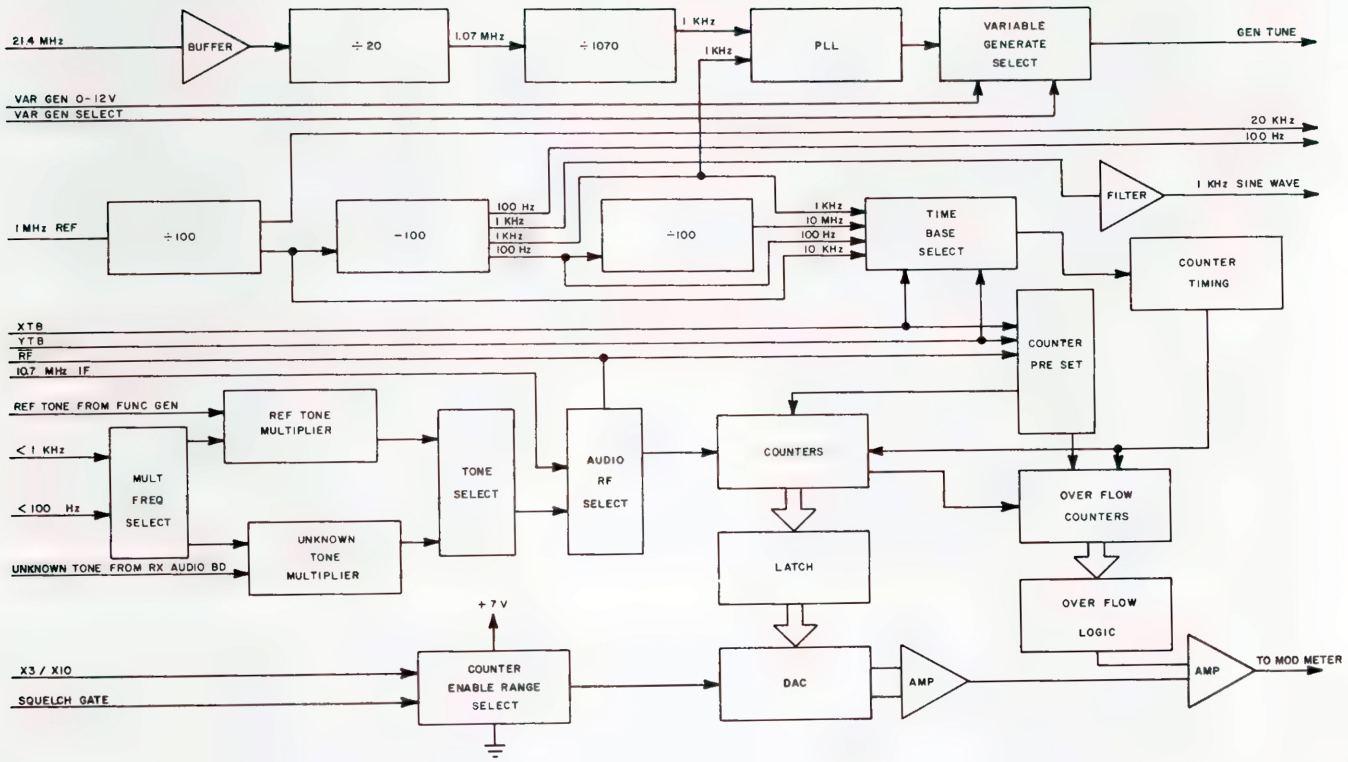


Figure 2-13 Digital Module Block Diagram

A. DIVIDERS

The 1 MHz signal enters the module at J4503 and is first divided by U4505 to produce 20 kHz (duplex REF Freq) and 10 kHz which is fed to U4506. U4506 divides the 10 kHz down to 1 kHz and 100 Hz. The 100 Hz is fed to U4507 where it is divded down to 10 Hz.

The 10 kHz, 1 kHz, 100 Hz, and 10 Hz are fed to multiplexer U4508 for time base selection for the digital counter. Selection of the time base is made by two control lines (XTB, YTB) from the Interface PC Board.

YTB	XTB	TIME BASE
LOW	LOW	10 Hz
LOW	HIGH	100 Hz
HIGH	LOW	1 kHz
HIGH	HIGH	10 kHz

B. PLL (PHASE LOCK LOOP)

The 21.4 MHz signal from the 10.7 MHz Gen/Rec Module, enters the Digital Module at J4502. First the signal is inverted by Q4501, then divided by 20 in U4501. This 1.07 MHz signal is fed to U4502 and divided by 1070 to produce a 1 kHz signal. This 1 kHz signal is fed to U4503, a phase lock loop, and compared with the 1 kHz REF signal from divider U4506 to produce a steering voltage for the 21.4 MHz Oscillator on the 10.7 MHz Gen/Rec Module. This steering voltage is fed to the analog multiplexer circuit, U4504. A variable DC voltage is also sent to U4504 from the front panel GEN/LOCK Control. When the variable GEN/LOCK Control is in the detent position, the VAR GEN enable line is low, which selects the steering voltage from the PLL chip, U4503 and passes this signal to the Gen Tune line. When the variable GEN/LOCK Control is out of detent, the VAR GEN enable line is high, which selects the DC voltage from the Front Panel Variable GEN/LOCK Control and passes it to the Gen Tune Line.

C. TONE MULTIPLIERS

Because the audio frequencies are too low for counting to the required accuracy within the available time base periods, both the reference and unknown frequencies are multiplied by a factor of 100 by separate phase locked loop circuits. The incoming tones are applied to the reference signal pin of the appropriate PLL (Phase Locked Loop) (U4510 for the unknown, U4512 for the reference). The VCO output from the PLL is divided by 100 by a counter (U4511 for the unknown, U4513 for the reference) and applied to the comparator pin of the PLL. The output of each loop is then applied to U4518. To inhibit the loop functions during the RF mode, Q4502 allows a +12V potential to inhibit operation of U4510 and U4512. When the audio mode is selected, the high mode select signal turns on Q4502, grounding the +12 potential, allowing U4510 and U4512 to operate.

D. SINEWAVE FILTER

A 1 kHz squarewave signal from the time base divider is filtered by a three-stage active filter consisting of op amps U4514 and U4515, and related components. The output of the filter is a 6 Vp-p sinewave supplied to the Generate Audio Module as the fixed tone signal.

E. PRESET LOGIC

Quad NOR gate U4414, quad NAND gate U4416 and hex inverter U4417 form a logic network to preset the counter system for a 1, 10 or 100 multiplier, according to the position of the FREQ ERROR Meter Control (X1/X3 selection is in the meter divider circuit). These presets are loaded into the counters during the 15 µS output pulse from U4413B (for audio frequencies, the preset count is zero).

F. SIGNAL SELECT CIRCUIT

Multiplexer U4401C couples the demodulated IF carrier from the 10.7 MHz Gen/Rec Module directly to the counter system when an RF position is selected on the FREQ ERROR Meter Range Control. When an audio position is selected, the Q output of U4412B alternately selects the reference frequency from the Variable Tone Generator, then the unknown demodulated audio frequency from the 10.7 MHz Gen/Rec Module. The selected signal is then coupled by U4401A to the counter circuit.

G. COUNTER TIMING CIRCUIT

The timing circuit consists of binary/decade counter U4411, dual D-type flip-flop U4412, multiplexer U4401B, inverter U4421E and dual one-shot multi-vibrator U4413. The input to the timing circuit is the selected time base frequency from multiplexer U4508. One output operates audio select multiplexer U4413 in the signal select circuit; other outputs control the counter circuit.

U4411 receives and counts the time base pulses. Starting with a high Q state of U4412A, when pin 2 of U4411 (representing binary 8) goes high, U4411 clocks U4412A to low Q. This produces a high output from U4421E, which clocks U4412B, and, simultaneously, provides a spike through C4413. The spike preloads a count of seven into U4411, overriding its count and pulling pin 2 back low. The next time base pulse causes pin 2 to again go high, clocking U4412A back to high Q. Pin 2 stays high for one more count, then goes low for the next eight counts. With the following pulse, the cycle repeats.

The high Q from U4412A inhibits the counter system for one time base period and is available to U4401B. When the $\overline{Q}$ output of U4412B is high, it is also available to U4401B. With the FREQ ERROR Meter Range Control in an RF position, U4401B selects the $\overline{Q}$ from U4412A; in an AUDIO position, it selects the $\overline{Q}$ from U4412B. The leading edge of the signal, as $\overline{Q}$ goes high, clocks U4413A, producing, as its output, a 15 µS low Q. As U4413A output $\overline{Q}$ returns high, it is applied to the counter circuit latch components and it clocks U4413B. U4413B now produces two 15 µS pulses--a high $\overline{Q}$ and a low $\overline{Q}$. These signals reset the counter system and U4412B. In the audio mode, U4412B has already been clocked to high $\overline{Q}$; however, in the RF mode, it has just been clocked to a high $\overline{Q}$, and is now, just a few microseconds later, clocked back to high $\overline{Q}$. The counter system counts upward when U4412B Q is low and downward when Q is high. This allows the counters to count upward on the audio reference frequency while Q is low, then downward on the unknown audio frequency while Q is high (while in the audio mode), but allows them, when in the RF mode, to only count upward.

H. COUNTER CIRCUIT

The counter circuit contains binary counters U4402 through U4406, dual D-type flip-flop U4407, latch U4408 and related gates and inverters. U4402 and U4403, the two least significant digit counters, furnish the meter deflection count, while U4404, U4405 and U4406 are overrange counters. If any terminal count in the latter is not zero, the meter will be pegged.

The selected frequency is applied to U4402 through U4401A. During loading, $\overline{Q}$ of U4412A and U4412B are high, which inhibit U4402 and U4403. When U4412A is clocked by U4411, successively clocking U4412B, the counters are allowed to count upward from preset values for a period of 10 time base pulses. The binary counts from U4402 and U4403 are applied to latch U4408 to drive the meter. Any non-zero count from U4404, U4405 or U4406 is applied through gates U4410, U4415B, U4420C and U4420D to either U4407A (if U4406, Pin 2 is low) or U4407B (if U4406, Pin 2 is high).

When the tenth time base pulse arrives, U4412A is clocked to a high Q state. In the RF mode, this inhibits the counter chain and initiates the end-of-count process. In the audio mode, it inhibits the counter chain while U4412B sets the counters to count down and changes the signal from the reference to the unknown frequency. The counters then count downward for the next ten time base pulses, then U4412A is again clocked to a high $\overline{Q}$ state. Now the end-of-count process is initiated for the audio mode.

The end-of-count process starts when U4413A is clocked by either U4412A or U4412B, and its $\overline{Q}$ output goes low for 15 µS. As $\overline{Q}$ goes high, U4408 is clocked, latching the count from U4402 and U4403 to DAC U4409. Simultaneously, U4407A and U4407B are clocked, and if any output from U4404, U4405 or U4406 is high, resulting from a frequency error that exceeds meter capacity, U4407A or U4407B will apply a high potential to the meter driver circuit. As $\overline{Q}$ of U4413A returns high, it also clocks U4413B, resulting in a 15 µS pulse output in which Q goes high and $\overline{Q}$ goes low to preload the counters from the logic network. Exclusive NOR gates U4418C and U4418, and inverters U4421C and U4421D prevent unwanted clocking of U4403, U4404, U4405 and U4406 during loading. With the next time base pulse, U4412A is clocked to high Q, low $\overline{Q}$, and the counting process repeats.

Inverter U4421A applies a high to the clear-direct pins of U4407A and U4407B when the RF signal is insufficient to break squelch, which prevents any possibility of overrange meter deflection.

I. METER DRIVER CIRCUIT

The meter driver circuit containing 8-bit DAC U4409, dual OP amp U4419, multiplexers U4504A and U4504C, and associated components.

When U4408 is clocked, it transfers the final count from U4402 and U4403 to the DAC. The two current outputs from U4409 are applied to op amp U4419, which is configured as a current-to-voltage converter. Trimpot R4407 allows calibrating the input level to U4419 to produce a zero output voltage when a count of 128 is applied to U4409. The output voltage of U4419 is positive or negative, depending upon which output from U4409 draws the higher current. U4419 inverts the output of U4409 and provides a 10:1 gain to drive the meter and provide for the digital readout. When the frequency error exceeds meter capacity, either U4407A or U4407B applies a high to the corresponding input of U4419B to peg the meter.

The reference voltage for the DAC is established by R4508 and trimpot R4510 for the X1 scale of the Frequency Error Meter, and by trimpot R4509 for the X3 scale. Multiplexer U4504B selects the scale, depending upon the setting of the FREQ ERROR Meter Range Control. When the carrier signal level is insufficient to break squelch, multiplexer U4504C couples the input of U4504B to ground. When the signal breaks squelch, U4504C then applies +6.9V to U4504B.

2-4-7 FUNCTION GENERATOR PC BOARD

The function generator produces six different tone configurations (sinewave, ramp, triangle, square, DTMF and pulse), a separate squarewave for audio error measurements, and three separate lines which indicate generated tone range (<100 Hz, <400 Hz and <1 kHz).

The tone output is fed to the front panel VAR Tone Selector Switch for use as either a modulation source on the Generate Audio PC Board or to the internal speaker for aural monitoring. The <100 Hz and <1 kHz signals are fed to the Digital Module, and the <400 Hz signal is fed to the Receive Audio PC Board.

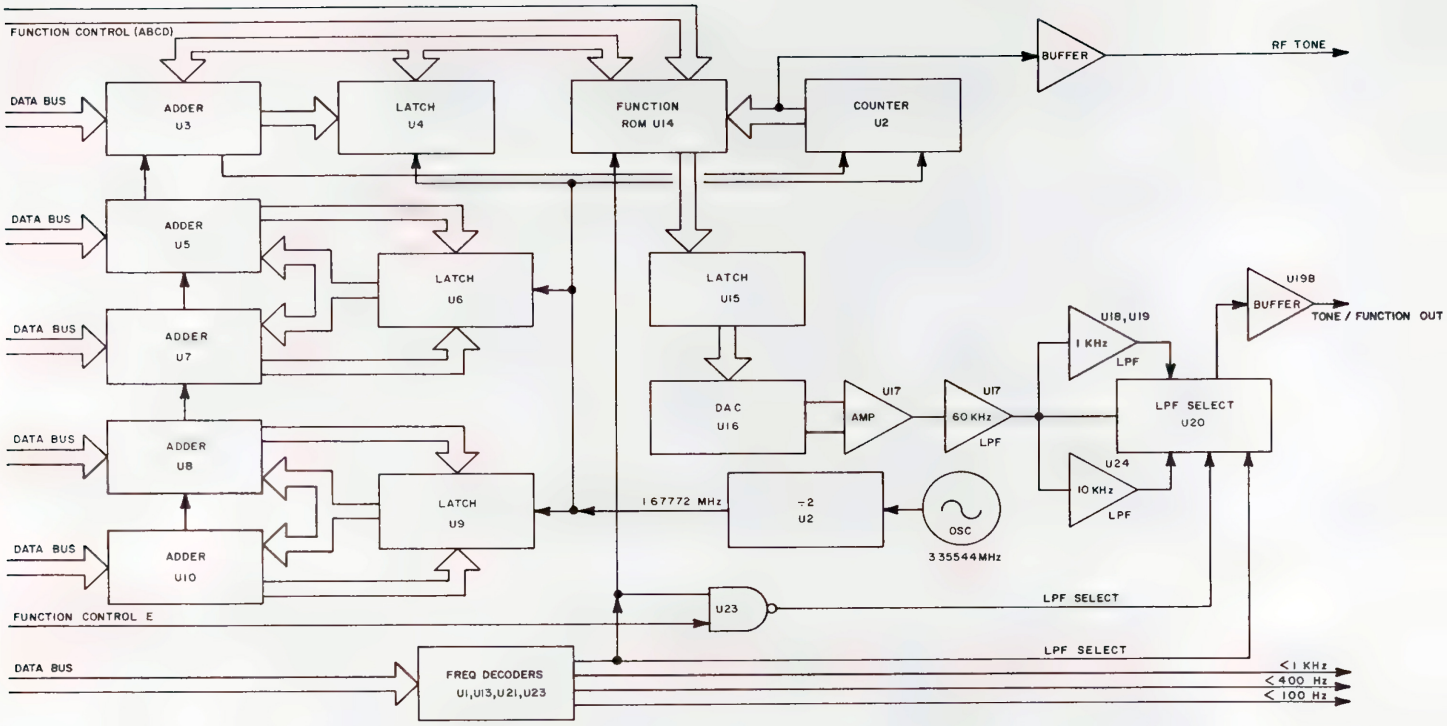


Figure 2-14 Function Generator PC Board Block Diagram

A. OSCILLATOR CIRCUIT

The reference oscillator contains 3.35544 MHz crystal Y3101, Q3102, trimcap C3110, and associated components. Q3101 buffers the signal, which then clocks binary counter U3102A. U3102A divides the frequency to 1.67772 MHz to clock the latches in the adder system.

B. ADDER SYSTEM

The adder system contains 4-bit binary adders U3103, U3105, U3107, U3108 and U3110, latches U3104, U3106 and U3109, and counter U3102B. One counter and one-half of a latch form a loop in which the data from the CPU and any carry-in from another adder are added to the output data from the latch, with the sum becoming the input to the latch. When the latch is clocked by the oscillator, the sum becomes a new latch output, which creates a new sum for the adder. The carry-out is chained to the next adder, and the process continued until the carry-out from U3103 is applied to U3102B. The 4-bit output data from U3102B and the three most significant bits from U3104 provide 128 binary codes which are applied to addresses 1 through 7 of ROM U3114. The most significant bit from U3102B is also applied to the bases of Q3103 and Q3104. These transistors produce a +12V squarewave at the selected frequency to provide the reference tone to the audio frequency counter in the Digital Module.

C. ROM/DAC CIRCUIT

ROM U3114 is programmed to produce binary codes to synthesize sine, square, ramp and triangle waveforms at a frequency selected through the CPU. It also produces codes for a modified squarewave for digitally coded squelch and composite sinewaves for sixteen preset dual tones. Addresses 8 through 12 of the ROM select the waveform to be synthesized, and addresses 1 through 12, providing 128 distinct timing codes, determine the relative phase position in the waveform cycle. From this information, the ROM produces an 8-bit output code corresponding to the amplitude required for the selected waveform at the particular phase position. Latch U3115, which is an 8-bit flip-flop, stores this code. When the oscillator clocks the adder system, it also clocks U3115. This latches the stored code from the ROM to DAC U3116 while simultaneously the adder system advances ROM addresses 1 through 7 to the next phase position, producing a new ROM output code. The coded input to U3116 turns on selected voltage dividers in the DAC, drawing a corresponding current. R3102 and R3103 are load resistors for the two current outputs from the DAC and with the resistors in the DAC, function as voltage dividers for op amp U3117A. U3117A compares the two voltage levels and produces a single output. R3103, being tied to ground, establishes symmetry to ground for the output signal. The resulting output from U3117A is an instantaneous voltage level corresponding to the amplitude required for the selected waveform at that particular phase position. As the oscillator continues clocking the adder system and the latch, the output voltage continues to change, describing the waveform throughout its cycle.

The signal from the ROM/DAC circuit passes through a two-stage 60 kHz low pass filter consisting of U3117B, U3118A, and associated components. The signal is then sent to a 10 kHz low pass filter, 1 kHz low pass filter and multiplexer U3120. The 10 kHz low pass filter is a two-stage filter consisting of U3124A and U3124B and associated components. The 1 kHz low pass filter is a two-stage filter consisting of U3118B and U3119A and associated components. The output of all three filters are fed to multiplexer U3120 for selection. The selected signal is then fed to U3119B, which buffers the signal, then to pin 9 of P2 to the front panel.

Function	Filter
Sinewave and DCS	
Less than 819.2 Hz	1 kHz
819.2 thru 13106.2 Hz	10 kHz
13106.2 Hz or Greater	60 kHz
Squarewave, Ramp, Triangle	
Less than 819.2 Hz	10 kHz
819.2 Hz or Greater	60 kHz
DTMF	1 kHz

Table 2-2 Tone/Filter Selection for Function Generator

D. FREQUENCY RANGE LOGIC

Because certain switching functions occur in the low pass filter circuit and Receive Audio and Digital Modules resulting from frequency selections, a logic network provides the appropriate data. This circuit consists of 4-input NOR gates U3111A, U3111B, and U3113B, 8-input OR/NOR gate U3121, and NAND gates U3123A and U3123B. The NOR gates read the binary when all corresponding code lines are low.

U3121 reads all code lines for 409.6 Hz and above, and when all are low, supplies a low output to U3101A and a high to the Receive Audio Module. If any code line goes high in response to a frequency selection, the outputs are reversed.

U3101A reads the code lines for 102.4 Hz, 204.8 Hz, 409.6 Hz and the non-inverting output from U3121. When all of these lines are low (selected frequency is below 102.4), the output from U3101A to the Digital Module is high.

When the output of U3113B is low (indicating a frequency of 13,106.2 Hz or greater), it pulls down on the control line to U3120A through CR3103. This output also provides one input to U3123B.

U3101B reads the code lines for 819.2 Hz, 1638.4 Hz, 3276.8 Hz and 6553.6 Hz. It provides the second input to U3123B.

When both input lines to U3123B are high (i.e., the selected frequency is below 819.2 Hz), the output from U3123A is high. This output goes to the Digital Module and to U3123D in the low pass filter circuit.

2-4-8 GENERATE AUDIO MODULE

The Generate Audio Module receives audio signals from any or all of four sources: (1) 1 kHz fixed tone from the Digital Module; (2) a variable tone from the Function Generator; (3) through the MIC/ACC Jack or (4) through the EXT MOD Jack on the Front Panel. These signals are combined and amplified, with a tap from the output going to the TONE OUT Jack. For FM modulation, the signal is sent directly to the 10.7 MHz GEN/REC Module 21.4 MHz VCO tuning line. For AM modulation, the signal is routed through an AM modulator/leveler, which consists of two amplifiers and the GEN LEVEL FINE Vernier Control, and then to the 10.7 MHz GEN/REC Module.

The operating mode (Generate or Receive) of other modules is determined by an operating mode circuit in the Generate Audio Module. In the Generate Mode, a GEN command (+12 VDC signal) performs the following functions: (1) it enables the generate amplifiers in the IF Module and Output Amplifier; (2) in the 10.7 MHz GEN/REC Module, it enables the frequency divider and inhibits the receive-enable multiplexer; and (3) in the Receive Audio Module, it enables the Modulation Meter multiplexer in the deviation/percent modulation mode. In the Receive mode, an REC command (+12 VDC signal) enables the receive amplifiers in the IF Module, and an ANT ENABLE command (+12 VDC signal) energizes the Antenna Enable Relay, coupling the signal between the Antenna Jack and the IF Module. If the set is operating in the Generate Mode and a signal exceeding 100 mW is received at the T/R Jack, it will automatically switch to the Receive mode, but the Antenna Enable Relay will not be energized. Also, with the set in the Receive mode, depressing the microphone Press-To-Talk Key automatically switches the set to the Generate mode and de-energizes the Antenna Enable Relay to route the generated signal from the IF block through the output amp.

The phase lock indicator circuit consists of four logic NAND gates (two of which function as an oscillator), a transistor in the Generate Audio Module, related grounding circuits in the High Loop and Low Loop Synthesizers, and the GEN/LOCK Control on the Front Panel. When the appropriate frequency in each Synthesizer is equal to and in phase with its reference, neither grounding circuit conducts and the voltages applied to the inputs of the first gate in the indicator logic circuit are high. When neither input to the gate is grounded, the transistor supplies 5V power to the LED on the Front Panel, indicating a phase-locked condition. If one or both inputs to the gate is grounded, or the GEN/LOCK Control is out of detent, the LED flashes, indicating an unlocked condition.

Audio signals from the Receive Audio Module low pass filters are also routed to the Generate Audio Module for DCS (Digitally Coded Squelch) decoding and SINAD/Distortion Analysis switching.

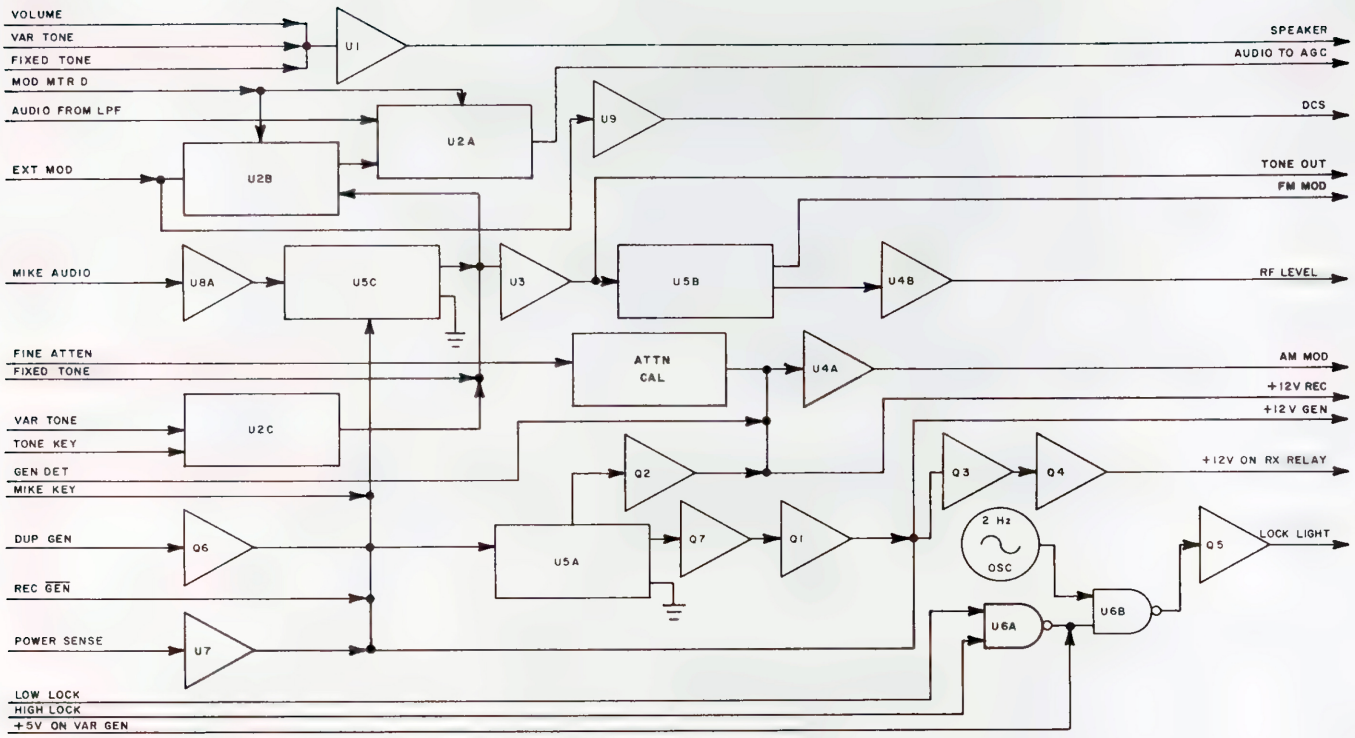


Figure 2-15 Generate Audio Module Block diagram

A. SPEAKER AMPLIFIER CIRCUIT

The demodulated audio from the Receive Audio Module, 1 kHz fixed toned from the Digital Module, and the tone from the Function Generator are combined in the Generate Audio Module and fed to audio amp U3201. U3201 amplifies the combined signals and sends it to the Speaker.

B. OPERATING MODE CIRCUIT

Transistor Q3201, which is a current limited transistor, supplies the generate enable voltage; Q3202 supplies the receive enable voltage; and Q3204, supplies the voltage to energize the antenna relay. The voltage applied at pin 11 of multiplexer U3205 controls these transistors. Op amp U3207 also controls Q3203 and Q3204.

When pin 11 of U3205 is low (generate or duplex generate mode is selected or microphone Press-To-Talk Key is depressed), pin 12 conducts through pin 14 to ground, turning on Q3207 and, subsequently, Q3201. This applies +12V to enable the generate function and to the base of Q3203. Q3203 is turned off, which turns off Q3204, and interrupts power to the antenna relay. The de-energized relay then conducts the RF signal from the IF Module to the Output Amplifier Module.

When pin 11 of U3205C is high, (receive mode is selected), pin 13 conducts through pin 14 to ground, turning on Q3202. Q3202 applies +12V to enable the receiver functions and to drive the AM modulator/leveler circuits to maximum attenuation of the signal generator VCO output in the 10.7 MHz Gen/Rec Module.

The power monitor in the Receive Audio Module furnishes a positive voltage to pin 3 of op amp U3207. This voltage level is proportional to the strength of any RF signal received at the T/R Connector. With no voltage applied to pin 3, the output at pin 6 is low, pulling down the bias voltage on Q3203, turning on Q3204 and energizing the antenna relay. This couples the ANTENNA Connector into the IF Block. If an RF signal exceeding 100 mW is applied at the T/R Connector, the voltage on pin 3 of U3207 goes higher than on pin 2, and the output at pin 6 goes high. Q3203 and Q3204 are turned off, the antenna relay is de-energized, and the received signal from the T/R Connector is coupled into the IF Block. The high output from pin 6 of U3207 is also applied to pin 11 of U3205C. This will cause U3205C to switch to receive mode if generate is selected, but will not override duplex generator or the microphone key.

When Duplex Generate Mode is selected, a high turns on transistor Q3206, which pulls down on pin 11 of U3205C, selecting the generate mode regardless of any signal applied at the T/R Connector.

C. AUDIO SWITCHING CIRCUIT

All audio signals supplied to the Generate Audio Module for modulation are combined and applied to pin 6 of op amp U3203B. The 1 kHz fixed tone goes directly to the amplifier. Signals from the microphone, Function Generator, and any signal applied thru the EXT MOD/SINAD Connector first go through switching circuits. The microphone Press-To-Talk Key pulls down on pin 9 of multiplexer U3205B, coupling the microphone audio signal at pin 4 to pin 5, then to the amplifier. The Function Generator signal at pin 3 of multiplexer U3202C is normally coupled to pin 4, then to the amplifier. When pin 9 of U3202B is pulled low, the Function Generator signal is interrupted.

The output from pin 1 of U3203A goes to the TONE OUT Connector on the Front Panel and to pin 15 of demultiplexer U3205A. When FM is selected, on the MODE Selector Control on the Front Panel, pin 10 of U3205A is low, and the signal at pin 15 is applied throuh pin 2 to the 10.7 MHz Gen/Rec Module. Selecting an AM mode applies a high to pin 10, coupling the signal on pin 15 to pin 1 and applying it to pin 6 of modulator/leveler op amp U3204B.

D. MODULATION CIRCUIT

The output of op amp U3204B (pin 7) goes to the Generate Level FINE Vernier Control on the Front Panel. Trimpot R3246 calibrates the control for -12 dB attenuation. From the potentiometer wiper, the signal returns to trimpots R3224 and R33227 for calibration. From R324, the signal is applied to pin 2 of op amp U3204A and applied to the AM modulator circuit in the 10.7 MHz Gen/Rec Module. The generate level signal from the Output Amplifier is summed with the modulating signal at pin 2 of op amp U3204A, providing a positive offset proportional to the RF level detected by the Output Amplifier. Accordingly, this biases the output of op amp U3204A and increases attenuation in the AM modulator circuit of the 10.7 MHz Gen/Rec Module until the RF level, at the level detector in the Output Amplifier, is 0 dBm. When the FM/AM-1200 is in the Receive or Duplex mode, the +12V output from transistor Q3202 is summed with any modulation signal applied to pin 2 of op amp U3204A. This voltage drives the output at pin 1 to -12V, which causes the AM modulator circuit to maximum attenuation and blanks out the generator VCO signal in the 10.7 MHz Gen/Rec Module.

E. PHASE LOCK INDICATOR CIRCUIT

Two NAND gates U3206C and U3206D, resistors R3242 and R3243, and capacitor C3218 form a 2 Hz oscillator. The oscillator output from U3206D pin 11 is applied to pin 5 of U3206B.

As long as approximately +5 VDC is applied to pins 1 and 2 of U3206A, the output on pin 3 remains low. If either the High Loop or Low Loop is not phase-locked to the appropriate reference frequency, one of the inputs goes low, and pin 3 goes high. While pin 3 is low and the GEN/LOCK Control is in LOCK, the input to pin 6 is a constant low, making the output at pin 4 a constant high. When the input to pin 6 is high, the oscillating input to pin 5 causes the output at pin 4 to oscillate. The high output from pin 4 turns on transistor Q3205 to supply +5 VDC, either steady or pulsing according to the high or low state of pin 4 of U3206, to the LOCK Lamp LED on the Front Panel.

F. DCS CIRCUIT

The LPF audio signal is routed to the DCS decoder U3209. If DCS is present in the RX audio signal, U3209A will detect it and U3209B will send the signal to the Interface PC Board.

2-4-9 10.7 MHz GEN/REC MODULE

In the Generate mode, the 10.7 MHz Gen/Rec Module utilizes a VCO tuned to 21.4 MHz to provide the carrier for RF signal generation. The output of the VCO is sampled by the Digital Module, which returns an analog tuning voltage to maintain the frequency at 21.4 MHz. When FM modulation is required, an audio modulation voltage from the Generate Audio Module is combined with the tuning voltages to produce the frequency modulated VCO output signal. A flip-flop divides the VCO output signal in half to produce the 10.7 MHz signal. This signal passes through an attenuator which, in the Generate AM mode, modulates the carrier with the audio modulation voltage from the Generate Audio Module. The signal is then sent to the IF Module and to the receiver circuit to allow the Receive Audio Module to monitor and display the signal on the Modulation and Frequency Error Meters.

In the Receive mode, the 10.7 MHz signal from the IF Module is fed to the receive enable circuit, two AGC controlled amplifiers, and one of three bandpass filters. These filters have a center frequency of 10.7 MHz with bandwidths of 200 kHz (FM Wide and Mid), 15 kHz (FM Narrow and AM Norm) and 6 kHz (AM Narrow and SSB). The signal is amplified again by a third AGC controlled amplifier, then demodulated, with the AM and FM audio going to the Receive Audio Module and the 10.7 MHz carrier going to the Digital Module. When in the Receive SSB Mode, a flip-flop divides the 21.4 MHz output of the VCO to 10.7 MHz and, through a BFO level potentiometer, injects the beat frequency into the modulated signal just ahead of the AM demodulator.

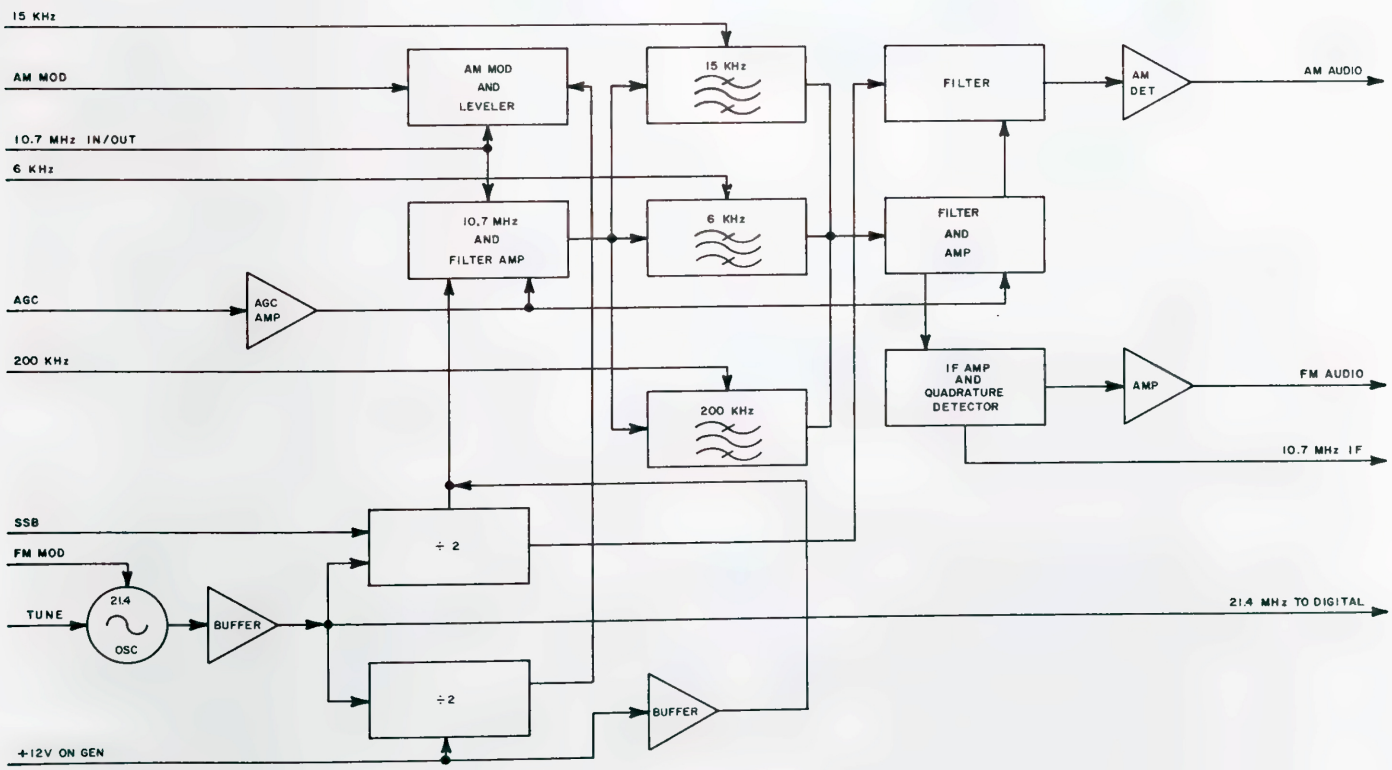


Figure 2-16 10.7 MHz GEN/REC Module Block Diagram

A. RECEIVE ENABLE/INHIBIT CIRCUIT

The 10.7 MHz IF signal from the IF Module first enters the receive circuit through J4302, diode CR4301 and tuned filter FL4301 to the bandpass amplifier. Resistor R4384 loads the circuit to prevent oscillation. A positive bias normally turns on CR4301. However, in the Generate mode, +12V is applied to the base of transistor Q4307. Q4307 grounds the bias voltage, turning off CR4301. Capacitor C4308 couples a sample of the generated signal into the receiver circuitry for monitoring.

B. BANDPASS AMPLIFIER CIRCUIT

The output from pin 3 of FL4301 is applied to the gate (pin 3) of FET Q4301. Filter FL4302 tunes the drain (pin 1) of Q4301 for the best AM envelope. The signal is then applied to the gate (pin 3) of FET Q4302. Filter FL4303 tunes the drain (pin 1) of Q4302 to 10.7 MHz. From FL4303, the signal is split and applied to three essentially identical bandpass filters.

Each filter consists of, in signal flow order, a blocking diode, a crystal filter, a transistor amplifier, a second crystal filter, and a second blocking diode. Diodes CR4308 and CR4312, 200 kHz crystal filters YFL4305 and YFL4306, RF transistor Q4310, and associated circuitry form the FM WIDE and FM MID filter; diodes CR4302 and CR4303, 15 kHz crystal filters YFL4301 and YFL4302, RF transistor Q4308, and related components form the FM NAR and AM NORM filter. The AM NAR and SSB filter consists of diodes CR4305 and CR4306, 6 kHz crystal filters YFL4303 and YFL4304, RF transistor Q4309, and affiliated components. To select one filter, a +12 VDC bias is applied to the two diodes and the collector of the transistor by the Front Panel MODE Selector Control, allowing the signal from FL4303 to reach pin 1 of the first crystal filter. The other two filters are then reverse biased with -5V to prevent conduction. The filter output at pin 3 is applied to the base of the transistor, producing the input to pin 1 of the second crystal filter. The output of the second filter at pin 3 then passes through the second diode of filter FL4304. From FL4304, the signal is coupled by capacitor C4319 to the gate of FET Q4311. The drain of Q4311 is applied through filter FL4305 to the AM and FM demodulator circuits.

Transistors Q4303 and Q4304 control the gain of FETs Q4301, Q4302 and Q4311. As long as the AGC voltage from the Receive Audio Module signal control circuit is positive, the FETs apply maximum gain to the IF signal. As the AGC voltage becomes increasingly negative, Q4303 and Q4304 pull down proportionately on the voltage applied to the input gates of the three FET's, thus reducing their gain.

C. AM DEMODULATOR CIRCUIT

The output from pin 2 of FL4305 is AC coupled through capacitor C4328 to the base of RF transistor Q4312. When the SSB mode is selected a 10.7 MHz BFO signal from the signal generator is also injected through inductors L4308 and L4309 and capacitors C4328, C4329 and C4331 to the base of Q4312. Q4312 and associated components amplify the signal, which is coupled through tuned filter FL4307 to an AM detector consisting of diode CR4304 and capacitor C4327. A bias voltage, supplied through resistor R4374, capacitor C4330, diode CR4315, and FL4307, keeps CR4304 turned on sufficiently to demodulate the signal linearly. The demodulated audio signal, applied to pin 5 of op amp U4303, is buffered by U4303 and associated components. The output at pin 7 is filtered by choke L4305 and capacitor C4344, then routed to the Receive Audio Module.

D. FM DEMODULATOR CIRCUIT

The output from pin 4 of FL4305 is AC coupled through capacitor C4377 to the base of RF transistor Q4313. Q4313, limiting diodes CR4317 and CR4318, and associated components form a limiting amplifier which strips off any AM and amplifies the remaining signal. The signal is then applied to pin 4 of U4302. U4302 is an IF amplifier with quadrature detector.

Resistor R4378, choke L4320, and capacitors C4341, C4342 and C4380 form a tuned circuit for the detector. One output from pin 1 of U4302 is the demodulated FM audio. The IF carrier, at 10.7 MHz, is routed from pin 9 to the Digital Module through J4303.

E. SIGNAL GENERATOR

FET Q4305 and related timing components produce a frequency of 21.4 MHz. As the tuning voltage is varied by the Variable GEN Control on the Front Panel, the oscillator frequency varies a minimum of 10 kHz above and below 21.4 MHz. Variable choke L4312 adjusts the frequency to 21.4 MHz at 4.80 VDC, which is mid range of the GEN Control travel. Diode CR10 is an AGC for the oscillator. After filtering by capacitor C4362, inductor L4319 and resistor R4362, the signal is buffered by transistor Q4306, then AC coupled through capacitor C4357 to J4304, and routed to the Digital Module for phase locking to the Frequency Standard. The Digital Module then produces the tuning voltage for phase locking the oscillator, or switches the variable generator tuning voltage to the oscillator when the GEN Control is out of the LOCK detent. In the FM mode, the modulating voltage from the Generate Audio Module is applied through pin 16 of J4301 to varactor CR4309.

The output signal from the VCO circuit at Q4306 is applied to pins 3 and 11 of dual flip-flop U4301. When SSB is selected, +12 VDC applied at pin 1 of U4301A allows the 21.4 MHz signal at pin 3 to clock the flip-flop, which produces a 10.7 MHz output at pin 5 (Q). Trimpot R4351 permits adjustment of the output (BFO) level. The signal is then applied to the AM demodulator circuit. When the generate function is selected, +12 VDC is applied to pin 13 of U4313. This allows the 21.4 MHz signal at pin 11 to clock the other flip-flop, producing a 10.7 MHz output at pin 9 (Q).

F. AM MODULATOR/LEVELER CIRCUIT

A filter consisting of capacitor C4368 and C4369, and choke L4314 shapes the square wave from pin 9 of U4301 into a sine wave. Diodes CR4313 and CR4314, chokes L4315 and L4316, capacitor C4370 and resistors R4352 and R4353 form a voltage controlled attenuator. The modulating/leveling voltage from the Generate Audio Module biases the diodes, varying the attenuation of the 10.7 MHz signal accordingly. From the modulator/leveler circuit, the 10.7 MHz signal is routed through J4302 to the IF Module.

2-4-10 HIGH LOOP MODULE

The Dual VCO difference frequency of 90-1088 MHz is divided by a number programmed by the RF selection, and the result is compared to the 500 kHz reference frequency from the Frequency Standard. A control circuit then steers the 1300-2298 MHz VCO to the frequency corresponding to the RF selection. Also, a second, rapid response control circuit steers the frequency of the 1210 MHz VCO to cancel noise produced by the 1300-2298 MHz VCO.

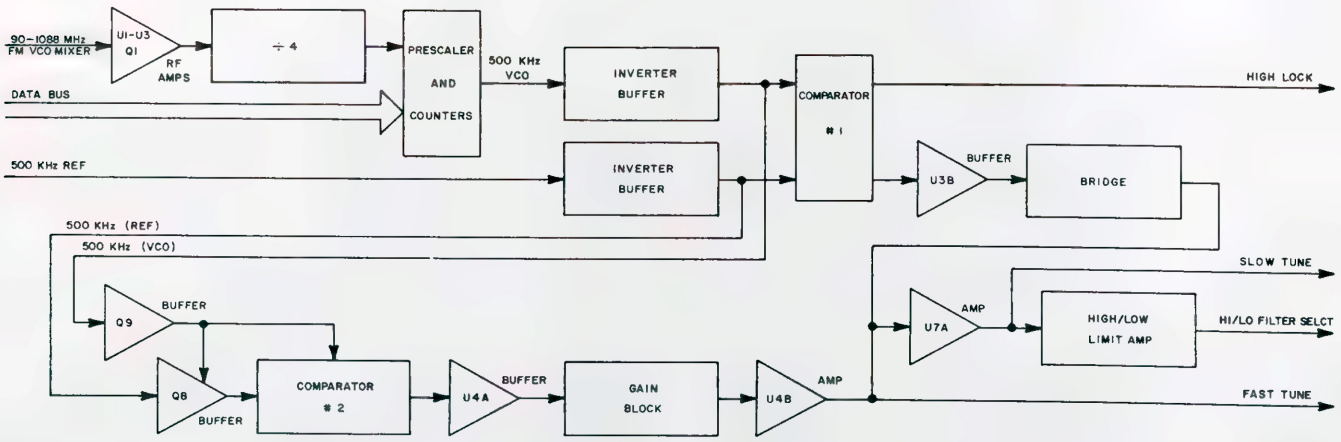


Figure 2-17 High Loop Module Block Diagram

A. SIGNAL AMPLIFIER

The 90-1088 MHz signal, produced in the dual VCO, is amplified by op amps U4101 thru U4103 and RF transistor Q4101. Capacitors C4108, C4111, C4114, C4121 and C4123 provide DC isolation of the inputs and outputs of the amplifiers, while RF chokes L4101 thru L4103 and associated capacitors prevent crosstalk through the power supply. L4104, C4124 and C4127 provide RF isolation of the amplifier circuit from the +12V power source. The amplified signal is applied to the programmable divider network and the Duplex Generator Module.

B. PROGRAMMABLE DIVIDER NETWORK

The programmable divider network divides the 90-1088 MHz signal by a selected number between 180 and 2176 to produce a 500 kHz output. It consists of prescalers U4104, and U4107, programmed counters U4105, U4106 and U4109, quad NOR gate U4108, dual flip-flop U4110, and associated resistors, capacitors and diodes.

BCD coding, initiated by the keyboard RF selection, loads the counter as follows: 2, 4 and 8 MHz sets U4105; 10, 20, 40 and 80 MHz sets U4106; and 100, 200, 400 and 800 MHz sets U4109.

The 90-1088 MHz signal from Q4101 is received by ÷4 counter U4104. U4104's output is then applied to ÷5/÷6 prescaler U4107, which clocks the three counters and U4110B. While a count is loaded into U4105, the output of U4108B is low, allowing U4107 to divide by six. When U4105 counts down to zero, U4108B goes high, and U4107 divides by five for the remainder of the counting period. U4108B, pin 5 also pulls up on pin 10 of U4105, stopping U4105 from counting until the next load cycle. U4107 will be forced to ÷5 during load operation as U4107, pin 2 is pulled high. U4105, U4106 and U4109 are programmed as down counters. When U4109 reaches zero count, the next clock pulse will bring pin 3 of U4109 high, clocking U4110. This brings pin 13 of U4108 low. When U4106 reaches count 7, pin 3 of U4106 will also go low bringing U4108, pin 9 low. As count 3 is reached, pin 20 of U4106 goes low. Pins 4 and 5 of U4108 are now both low, forcing pin 2 of U4108 high.

The next clock pulse (count 2) will clock U4110B, bringing Q (pin 15) high and $\overline{Q}$ (pin 14) low. U4110B $\overline{Q}$ loads counters U4105, U4106 and U4109. U4110B Q resets U4110A bringing $\overline{Q}$ high. This forces the Q input to U4110 low. The next clock pulse (count 1) will remove the load condition from U4105, U4106 and U4109, allowing them to count normally. It takes nine clock pulses from U4107 after U4109 reaches zero to reset the system. Pins 4 and 5 of U4107 take the ECL outputs of U4110A, pin 3 and U4110B, pin 15 and convert them to a TTL output at pin 7 of U4107. U4107, pin 7 should be 500 kHz.

C. FREQUENCY COMPARATOR CIRCUIT

The frequency comparator circuit compares the output frequency from the programmable divider network to a 500 kHz reference from the Frequency Standard. If the two squarewave signals are not synchronized, the comparator circuit produces an out-of-lock indication and an integrator provides steering voltage to the 1300-2298 MHz VCO integrator circuit.

The reference frequency is applied to the clock at U4002B and the controlled frequency to the clock of U4002A. U4002 is a dual, negative edge triggered flip-flop. Depending upon the phase relationship of the two signals, the flip-flops vary the voltage on C4006, the input to op amp U4003B, to produce a correction voltage. When the signals are in phase, R4019 and R4021 set the input voltage at approximately +2.5V, resulting in a correction voltage of approximately zero.

From reset of U4002, Q_A and Q_B are low, causing NAND gate U4018 output (to the reset of both flip-flop) to be high. $\overline{Q}_A$ and $\overline{Q}_B$ are high, causing the output of U4001D to be low. If both flip-flops are clocked simultaneously, U4001B instantly resets U4002A and U4002B, and capacitors C4005 and C4006 prevent any instantaneous systems responses. However, if one signal leads the other, the outputs of U4002A and U4002B will be opposites for the period of time one leads the other. This causes the output of U4001D to go high and allows the voltage applied to U4003B to be raised or lowered accordingly through CR4005 or CR4004.

With the output of U4001D high, Q4007 conducts, thus illuminating LED CR4106 on the divider board. It also pulls down on pin 2 of U3206A in the phase lock indicator circuit in the Generate Audio Module, causing the LOCK Lamp LED on the Front Panel to flash.

When the voltage on pin 5 of U4003B deviates from normal, the output voltage varies directly from zero. This voltage is then applied to a bridge consisting of diodes CR4008, CR4009, CR4010 and CR4011. Any positive or negative voltage from U4003B, exceeding two diode gaps from zero, is applied to the 1300-2298 MHz VCO integrator circuit to correct its frequency. The effect of the bridge is to delay shifting the 1300-2298 MHz VCO for detailed noise while allowing the 1210 MHz oscillator to make the necessary shift to cancel the noise.

D. 1300-2298 MHz VCO CONTROL CIRCUIT

An integrator circuit containing Q4012 and op amp U4007A controls the voltage level applied to the 1300-2298 MHz VCO. Op amps U4008A and U4008B, with trimpots R4060 and R4061, set the high and low voltage limits, thus establishing the low and high frequency limits at approximately 1275 and 2300 MHz respectively. Op amp U4007B, calibrated by trimpot R4065, establishes the switching frequency of the High/Low Pass Filter, and supplies either +12V or -12V as required.

E. PHASE COMPARATOR

The phase comparator circuit contains two sample and hold circuits to compare the phase relationship of the programmable divider output signal to the 500 kHz reference signal, and an integrator circuit to supply a correction signal.

In the first sample and hold circuit, the reference signal is buffered by Q4002, then applied to the emitter of Q4001 and the collector of Q4003. The controlled signal is applied to the base of Q4005, which applies a corresponding sampling pulse to the bases of Q4001 and Q4003. For the duration of this pulse, if the reference signal is high, Q4003 conducts and charges C4002; if the reference is low, Q4003 conducts, and discharges C4002. The net charge held by C4002 is proportional to the phase relationship of the two signals.

The voltage at C4002 is buffered and inverted by Q4004 and Q4008, then applied to the source of Q4011. The sampling pulse from Q4005 is coupled by a delay network consisting of Q4006 and Q4009. When the gate of Q4011 goes high, the voltage at the source is coupled to the drain and held by C4010. Q4010 supplies a pulse 180° out of phase with the gate pulse to Q4011. This pulse is calibrated by trimpot R4032 and coupled to C4010 to null 500 kHz transition noise. The voltage level at C4010 is applied to op amp U4004A. The gain of U4004 is such that when the two signals are synchronized, its output level is zero volts.

F. 1210 MHz VCO CONTROL CIRCUIT

In order for the phase comparator to make corrections over the entire span of the 1300-2298 MHz VCO, the control signal from U4004A must vary considerably. To maintain an adequate response of the 1210 MHz VCO, the gain of op amp U4004B is controlled by the RF selection. Switches U4005A, U4005B, U4005C, U4006A, U4006B and U4006C, enabled by frequency select control lines (40, 80, 100, 200, 400 and 800 MHz), select various resistances which, in conjunction with R4044 and trimpot R4045, establish the correct gain for U4005B. The output of U4005B is filtered, then routed to the 1210 MHz VCO in the Dual VCO. An attenuated control signal is also applied through R4046, to the 1300-2298 MHz VCO control circuit to coordinate frequency changes required to phase lock the programmable divider output frequency to the 500 kHz reference signal.

2-4-11 DUAL VCO MODULE

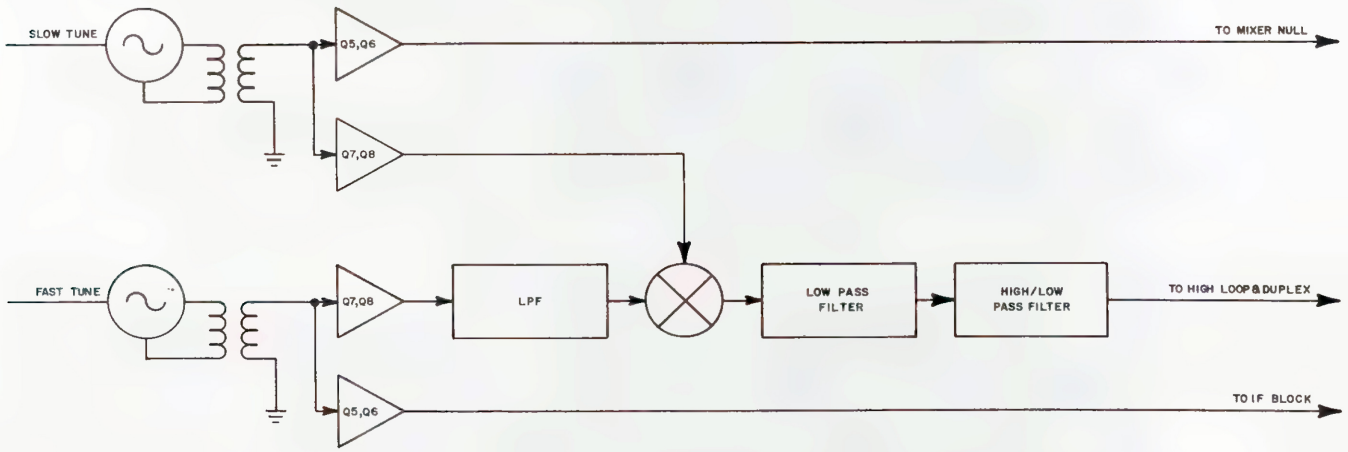


Figure 2-18 Dual VCO Module Block Diagram

The following theory of operation is provided to explain the interaction of the Dual VCO with other modules. It is not intended to provide sufficient theory for testing or repairing individual circuits within the module.

CAUTION

THE DUAL VCO IS NOT FIELD REPAIRABLE AND SHOULD BE RETURNED TO THE MANUFACTURER IF TESTS INDICATE THE MODULE IS FAULTY. ATTEMPTS TO REPAIR THE MODULE WITHOUT SPECIALIZED EQUIPMENT AND KNOWLEDGE CAN DRASTICALLY ALTER ITS CHARACTERISTICS AND CAUSE THE MODULE TO BE UNSERVICEABLE WHEN IT COULD OTHERWISE BE REPAIRED AT THE FACTORY.

The Dual VCO Module produces two of the three local oscillator frequencies required by the IF Module. These two frequencies are also mixed and their difference frequency is used by the High Loop Module in controlling the Dual VCO, and by the Duplex Module to produce the offset frequency when operating in the Duplex Mode.

The first VCO frequency is varied between 1300 MHz and 2298 MHz in 2 MHz increments by the High Loop in response to the megahertz portion of the RF selection (RF selection within each of the 2 MHz increments controls the Low Loop frequency). The second VCO frequency is tuned to 1210 MHz, but is inversely frequency modulated to cancel noise produced by the first VCO.

The two frequencies are mixed in the Dual VCO, with the mixed frequency being filtered by two external filters and applied to the High Loop Module, then to the Duplex Generate Module. The High Loop compares the difference frequency (90 MHz to 1088 MHz) to a standard frequency and produces the tuning voltage for the 1300-2298 MHz VCO and the frequency modulating voltage for the 1210 MHz VCO. The tuned VCO outputs are then applied to the IF Module.

2-4-12 1120 MHz LOW PASS FILTER

The 1120 MHz Low Pass Filter is a tubular, in-line filter tuned to attenuate all frequencies above 1120 MHz by at least 40 dB. This allows only the 90-1088 MHz difference frequency from the 1300-2298 MHz VCO and 1210 MHz VCO in the Dual VCO Module to reach the High/Low Pass Filter. The filter is tuned and sealed at the factory and is not field repairable.

2-4-13 HIGH/LOW PASS FILTER

The High/Low Pass Filter prevents harmonics of lower frequencies (which may pass through the 1120 MHz low pass filter) from interfering with the High Loop frequency comparator. The 90-1088 MHz signal from the 1120 MHz Low Pass Filter is received at J602. Depending upon whether the 10 VDC control signal from the High Loop is positive or negative, applied at FL601, diode switches route the signal through either a 450 MHz high pass filter or a 520 MHz low pass filter, respectively. The actual crossover frequency, established in the High Loop, varies from set to set, and is marked on the outside of each module calibrated at the factory.

2-4-14 LOW LOOP MODULE

A VCO in the Low Loop Synthesizer produces a frequency of 79.3 to 77.3001 MHz. The VCO signal is buffered, then split three ways. One output is applied to the Spectrum Analyzer, a second supplies the IF Module, and the third is used for VCO frequency correction. A divider network, programmed by the microprocessor, divides the VCO frequency by 793,000 to 773,001. A phase/frequency detector compares the resulting frequency with a 100 Hz reference from the Digital Module, and produces a steering voltage for the VCO.

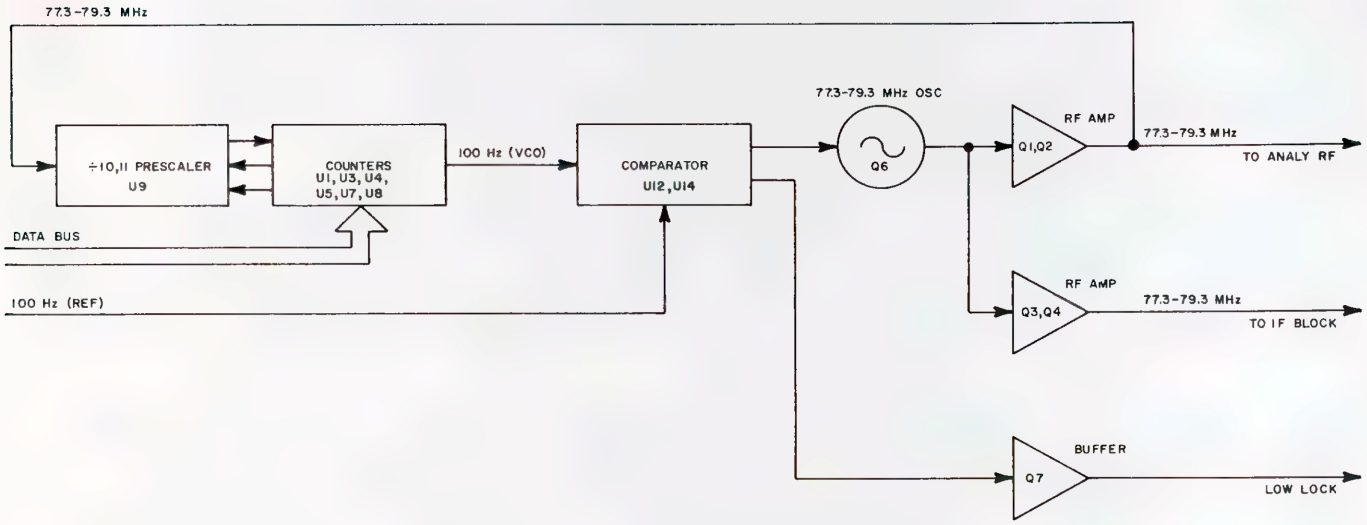


Figure 2-19 Low Loop Module Block Diagram

A. VCO CIRCUIT

The Low Loop output of 79.3 to 77.3001 MHz is produced by voltage controlled oscillator Q4206. Variable inductor L4203 provides calibration adjustment. Inductor L4202 and capacitor C4212 decouple the oscillator from the power supply circuitry. Oscillator tuning bandwidth is established by capacitors C4213, C4214 and C4217, inductor L4203, and diode CR4203. Diode CR4202, resistor R4217, and capacitor C4215 control the amplitude.

B. BUFFER AMPLIFIERS

The VCO output is buffered by transistor Q4205, then applied to the programmable divider network and two independent buffers. One second stage buffer, consisting of transistors Q4203 and Q4204, feeds the third mixer of the IF Module. The other second stage buffer, which uses transistors Q4201 and Q4202, furnishes a reference signal to the programmable divider network, and through J4203 to the analyzer RF module.

C. PROGRAMMABLE DIVIDER NETWORK

The programmable divider network consists of a ÷10/÷11 prescaler U4209, dividers U4201, U4203 thru U4205, U4207 and U4208. Dual flip-flop U4202, U4206, U4210 and U4211, and related components. The divider network divides the VCO frequency by a number preset by the processor. The output of the divider network (nominally 100 Hz) is fed to the phase/frequency detector circuit.

D. PHASE/FREQUENCY DETECTOR

The output from the divider network clocks flip-flop U4212A and the 100 Hz reference clocks U4212B. The corresponding Q outputs of the flip-flops are connected to pins 12 and 13 respectively of NAND gate U4213D, with the gate output from pin 11 applied to reset both flip-flops. The Q output of U4212A charges capacitor C4224 through diode CR4204. The $\overline{Q}$ output from U4212B discharges C4224 through CR4205. Thus, if the two input frequencies are in phase, the charge on capacitor C4224 stays constant. However, if the inputs are not in phase, the charge on C4224 is a DC correction voltage to pin 6 of op amp U4214B. U4214B and associated components form an integrator to supply the VCO steering voltage.

E. PHASE LOCK INDICATOR

Both $\overline{Q}$ outputs from pins 13 and 8 of U4212 are applied to pins 9 and 10 respectively, of NAND gate U4213C. When the divider output frequency at pin 1 of U4212A is not in phase with the reference frequency at pin 5 of U4212B, pin 8 of U4212B goes high, turning on transistor Q4207. Q4207 then grounds LED CR4207 to indicate the Low Loop is not phase-locked, and pulls down pin 1 of the phase lock indicator gate, U4211A, on the Generate Audio Module, causing the Front Panel LOCK Lamp to flash.

2-4-15 NULL MIXER ASSEMBLY

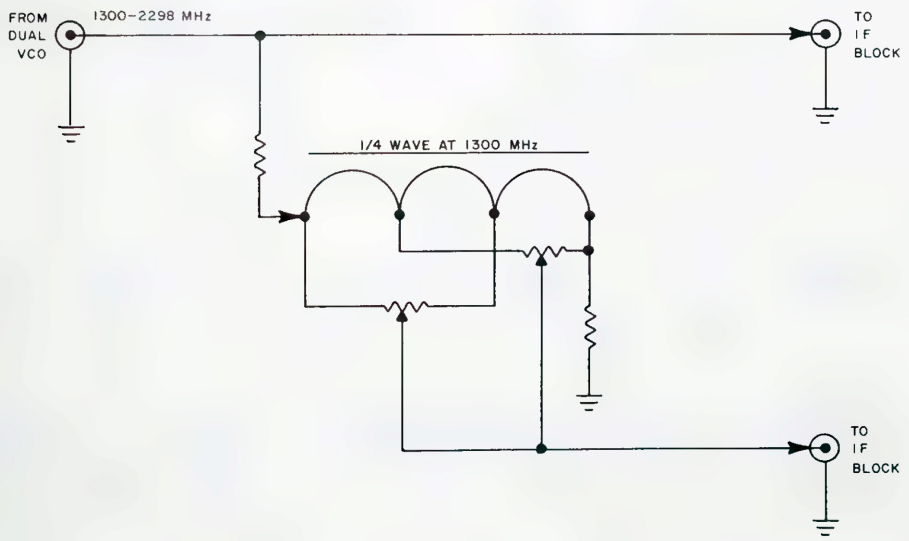


Figure 2-20 Null Mixer Assembly Block Diagram

The Null Mixer Assembly rceives the 1300-2298 MHz signal from the Dual VCO Module, where it is teed, with one signal being fed directly to the first mixer in the IF Module, and the other being routed to a phase shift circuit, whose output is 180° out of phase with the first mixer. Trimpot R9402 selects an amplitude of the 1300-2298 MHz signal between the 0° and 180° points and Trimpot R9402 selects the signal amplitude between the 90° and 270° points. The two selected signal amplitudes are combined and fed to the IF Module where it is combined with the output of MXR9402. The level of this signal, as set by R9402 and R9403, reduces the IF frequency of 1300 MHz.

2-4-16 IF BLOCK ASSEMBLY

The function of the IF Module, in the Receive Mode, is to select the signal source, then convert the selected RF to 10.7 MHz IF and reject all other frequencies. In the Generate Mode, the IF Module converts the generated 10.7 MHz IF to the selected RF and directs the signal to the Output Amplifier. One low pass and two bandpass filters, three mixers, two amplifiers, and signals from three local oscillators accomplish this conversion. On Serial Numbers 1246 and after, a separate Null Mixer Assembly is installed to reduce the level of the zero pulse.

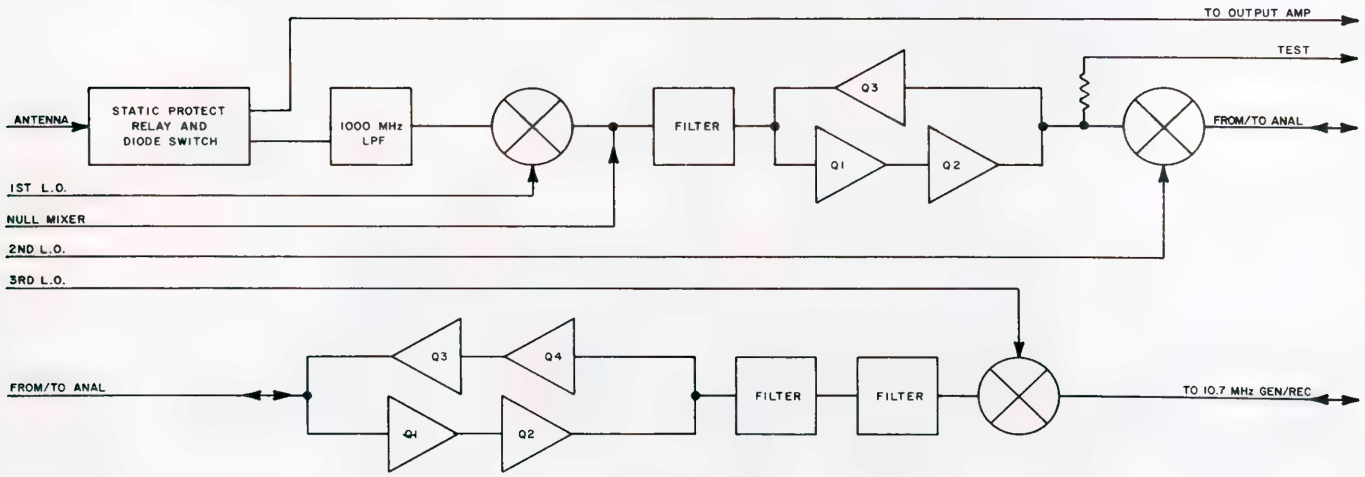


Figure 2-21 IF Block Assembly Block Diagram

A. RECEIVE MODE

An RF signal from the antenna, received at J2201, first passes through static protect and diode switch circuits. R3801, R3802, CR3801 and CR3802 form the static protect and R3803, R3804, C3801, C3802, CR3803 through C3806, L3801 and L3802 form the diode switch. When the +12V antenna enable command is applied to the antenna enable circuit, the two resistors maintain a forward bias on the diodes to conduct the RF signal, while the two capacitors isolate the DC from the RF circuits and the two inductors isolate the RF from the power supply circuits. Prior to S/N 1468, the signal from the diode switch is applied to antenna enable relay K3801. On SN 1468 and after, a constant gain amplifier is installed prior to relay K3801. The amplifier circuit consists of Q3801, C3803, C3804, and R3805 through R3808. The +12V antenna enable command activates the amplifier only when the antenna is selected.

The command also energizes the antenna enable relay, coupling the antenna circuit into the first IF mixer circuit. However, if the Receive Mode is selected and a signal is applied to the T/R Connector which exceeds 100 mW, power detector and switching circuitry interrupts the antenna enable command, switching the relay to couple the signal from the T/R Connector to the mixer circuit.

Low pass microstrip filter FL2211 limits the RF to less than 1000 MHz. MXR2202 then mixes the received signal with the 1300-2298 MHz signal from the Dual VCO. The mixer output is then combined with the noise cancellation signal from the Null Mixer Assembly. A 20 MHz bandpass filter at 1299 MHz, which consists of tuned cavities FL2205, FL2206 and FL2207, passes only the difference frequency. Q2401, Q2402 and associated circuitry form a 1300 MHz amplifier which is enabled by the +12V receive command when the Receive or Duplex mode is selected. MXR2201 then mixes this difference frequency with the 1210 MHz signal from the Dual VCO. The mixed signal is then routed through J2209 to the Spectrum Analyzer RF Module, where the signal is teed with one signal being returned to J2208 in the mixer circuit.

Upon its return from the Spectrum Analyzer RF Module, the signal is amplified by Q2203, Q2204 and related components, then filtered by FL2201, FL2202, FL2203, FL2301 and FL2302 to 88-90 MHz. MXR2301 then mixes the signal with the 79.3000 - 77.3001 MHz signal from the Low Loop Module. The resulting signal is then applied to the 10.7 MHz Gen/Rec Module.

B. GENERATE MODE

MXR2301 mixes the 10.7 MHz signal from the 10.7 MHz Gen/Rec Module with the 79.3000 - 77.3001 MHz signal from the Low Loop Module. FL2301, FL2302, FL2201, FL2202 and FL2203 then pass the sum frequency of 88-90 MHz. Q2201, Q2202 and related components amplify the signal before it is routed to the Spectrum Analyzer RF Module, where it is teed with one signal being returned to J2209 in the second IF mixer circuit.

MXR2201 mixes the signal returned from the Spectrum Analyzer RF Module with the 1210 MHz signal from the Dual VCO Module. The signal is then amplified by Q2403 and related components. Tuned cavity bandpass filters FL2205, FL2206 and FL2207 then pass the sum frequency of 1298 - 1300 MHz, which is then mixed by MXR2202 with the 1300 - 2298 MHz signal from the Dual VCO Module. 1000 MHz low pass microstrip filter FL2211 passes only the difference frequency, which is the selected RF. The signal is then routed through the unenergized antenna enable relay, K2201 or K3801, and J2202 to the Output Amplifier.

2-4-17 OUTPUT AMPLIFIER MODULE

In the Receive mode, the output Amplifier Module couples any signal received at the T/R Connector through a 20 dB pad, to the IF Module. In the Generate mode, it amplifies the signal received from the IF Module, and routes it to the Step Attenuator on the Front Panel. This signal is then returned to the Output Amplifier for 20 dB additional attenuation, and routed to the T/R Connector. In the Duplex mode, the signal from the Duplex Generator Module is routed through the 20 dB attenuator to the T/R Connector.

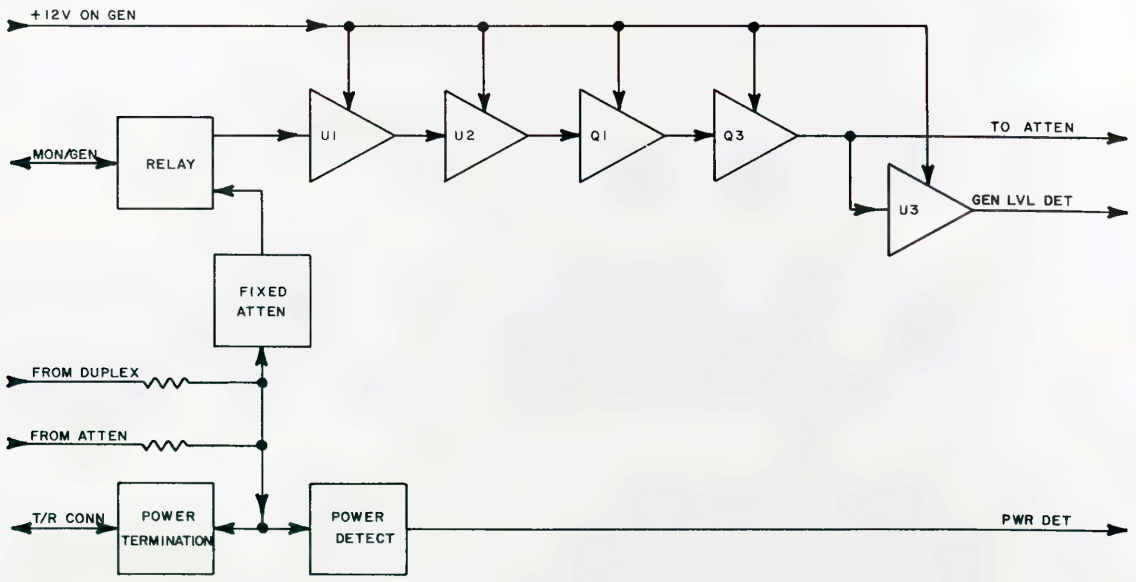


Figure 2-22 Output Amplifier Module Block Diagram

A. RECEIVE AND DUPLEX MODES

All signals received through the T/R Connector are attenuated 20 dB by RN5101. The signal is then teed, with one signal going to the power detector circuit, consisting of CR5108, C5124, trimcap C5127, L5107, R5128, R5134 and R5147. The detector circuit converts this signal to a DC voltage level corresponding to the signal power, and supplies the result to the Receive Audio Module. The other signal is further attenuated by a series of voltage dividers using R5135 through R5146, and coupled by relay K5101, through J5101, to the IF Module.

B. GENERATE MODE

In the Generate mode, +12V energizes mode relay K5101 and enables the generate amplifier and level detector circuits. The relay couples the RF signal from the IF Module to the amplifier circuit. Two amplifiers, U5101 and U5102, amplify the signal and apply it to the base of RF transistor Q5101 which, in turn, controls the base of RF transistor Q5103. Q5102 is a bias transistor to adjust the base current of Q5103 to achieve a constant collector current in Q5103. The signal level at this point is nominally 0 dB. From the collector of Q5103, the signal is coupled through J5103 to the GEN LEVEL Step Attenuator and through CR5102 to the generate level detector circuit.

The Step Attenuator, while not a physical part of the Output Amplifier Module, is electrically an integral component. It attenuates the generated signal from 0-100 dB in 10 dB steps, allowing operator control of the signal level. (Vernier control from +1 to -11 dB is achieved by varying the signal level in the Gen/Audio Module.) From the Step Attenuator, the signal is returned to the Output Amplifier, where RN1501 attenuates it an additional 20 dB. The signal is then routed to the T/R Connector.

CR5102 and C5116 form a level detector which senses the level from Q1503. Amplifier U5103 then sends an analog DC signal to the Generate Audio PC Board. The AM modulation circuit uses this signal to adjust the modulator/leveler attenuator in the 10.7 MHz Gen/Rec Module, thereby affecting the level of the generated signal which is ultimately applied to the Output Amplifier. Trimpot R5114 allows calibration of the output from U5103 as necessary, to obtain a level of 0 dB at J1503.

2-4-18 DUPLEX MODULE

To produce the duplex RF signal, the Duplex Module uses two local oscillators. The frequency offset command, received from the processor, adjusts one VCO frequency through the phase lock circuit. The modulated FM audio signal from the 10.7 MHz Gen/Rec Module modulates the other VCO frequency. The two output frequencies are mixed, with the difference frequency being mixed with the Dual VCO difference frequency. The final frequency is an FM signal at the selected RF plus or minus the selected offset frequency.

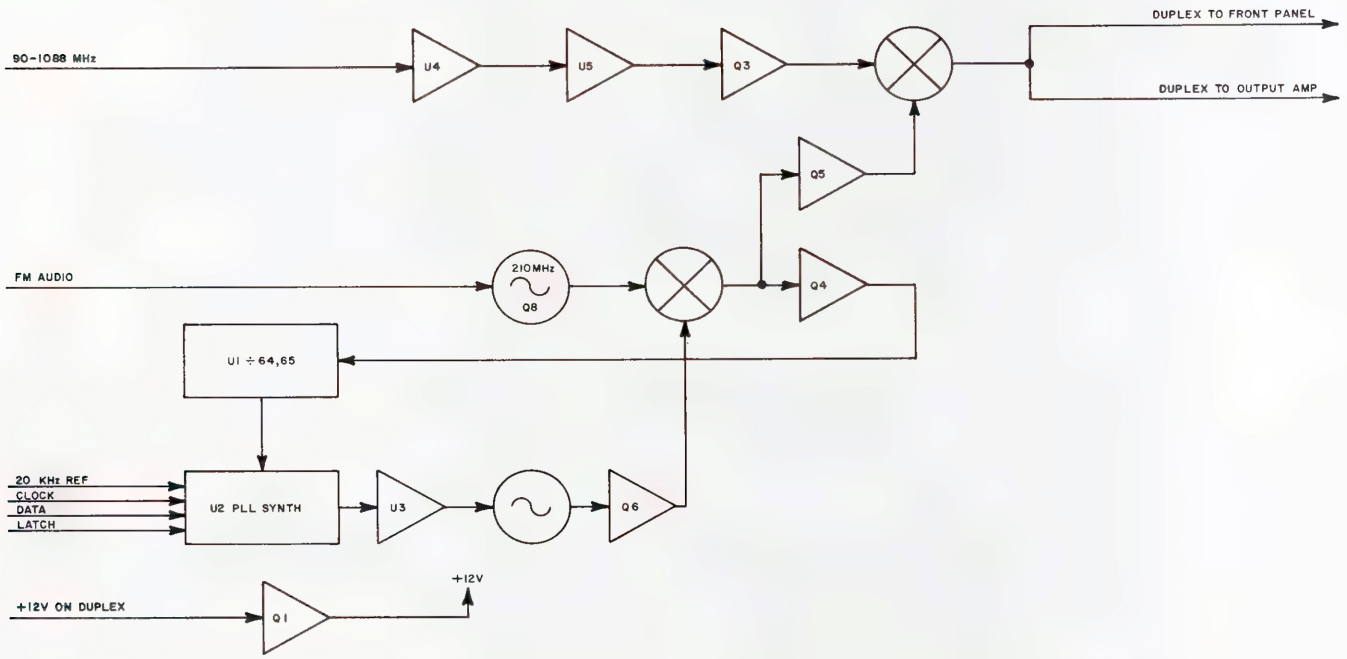


Figure 2-23 Duplex Module Block Diagram

A. SUBREGULATOR

The +12V VDC from the Power Supply is subregulated on the Duplex PC Board to operate the oscillators and phase lock network. Zener diode CR1205 establishes the reference voltage for op amp U1206A. The output of U1206A is applied to the base of transistor Q1502. The collector voltage from Q1502 is sampled by U1506A through a voltage divider consisting of trimpot R1251 and resistors R1552 and R1553. Thus, U1506A changes its output as necessary for Q1502 to hold the collector voltage at the level required to balance the voltages at the input pins of U1206A.

B. 250-350 MHz OSCILLATOR

The oscillator operating voltage is applied through RF choke L1212 to FETs Q1207 and Q1209. Varactor CR1202 and inductor L1211 form a tank circuit. The tuning voltage from the phase lock integrator U1203B, isolated through R1246 and L1215, establishes the frequency of the oscillator. Diode CR1204, installed between the source and the gate of the two parallel FETs, provides AGC for the oscillator. The output signal passes through RF choke L1210, and is coupled by C1258 to the base of Q1206. Q1206 amplifies the signal to approximately +7 dBm, then C1257 couples the signal to the LO port of MXR1202.

C. 210 MHz OSCILLATOR

The oscillator operating power of +11 VDC is supplied through R1222. Variable RF choke L1209 tunes FET Q1208 to 210 MHz. The modulated FM audio signal from the 10.7 MHz Gen/Rec Module is applied to varactor CR1201 to modulate the frequency of the oscillator. Diode CR1203, between the source and the drain of Q1208, provides AGC for the oscillator. RF choke L1208 provides circuit isolation, and L1207, L1213, C1242, C1243 and C1276 form a low pass filter. R1228 and R1229 form an impedance matching pad for the RF port of MXR1202.

D. OFFSET MIXER AND FILTER

Mixer MXR1202 combines the frequencies from the 210 MHz VCO and the 250-350 MHz VCO. The combined signal is then filtered by a 150 MHz low pass filter to pass only the difference frequency of 40-140 MHz. The filter consists of L1205, L1206, L1214, C1250, C1251, C1252 and C1277. From the mixer, the signal is applied to the phase lock circuit and the duplex mixer circuit.

E. PHASE LOCK CIRCUIT

The 40-140 MHz signal from the offset mixer and filter is coupled through C1249 to transistor Q1204. The amplified signal is coupled through C1248 to dual modulus prescaler U1201. As long as pin 1 is low, U1201 divides by 65; when the control line from U1202 pin 8 to U1201 pin 1 is high, U1201 divides by 64. The output frequency from U1201 is applied to the frequency input pin of U1202.

U1202 is a serial input PLL frequency synthesizer that divides the input frequency by a programmed number from the processor, compares the result with the 20 kHz reference from the Digital Module, and produces two VCO steering voltages. When the offset signal is at the selected frequency, both control voltages from pins 3 and 4 of U1202, are high. One pin will be low, depending upon phase relationship, when the offset frequency is not phase-locked to the reference frequency.

Both control voltages from U1202 are applied to an integrator consisting of op amp U1203B and associated components. R1216 with C1228, and R1217 with C1227 are differentiating circuits to shape the square wave control signals into basically sawtooth waves. R1220, C1229 and C1264 from the output of U1203B to pin 6, and R1221, C1226 and C1274 from pin 5 to ground, slow the phase lock response sufficiently to prevent cancellation of FM applied to the 210 MHz oscillator. The output of the phase lock circuit at pin 7 of U1203B is applied to the tuning circuit of the 250-350 MHz oscillator.

F. DUPLEX MIXER CIRCUIT

The 40-140 MHz offset signal, received from the offset mixer and filter, is amplified by Q1205. The output level is then calibrated by trimpot R1230 and applied to the IF port of MXR1201. The 90-1088 MHz signal from the High Loop is amplified by op amps U1204 and U1205 and transistor Q1203, and applied to the LO port of MXR1201. Power for the amplifiers is supplied by Q1201 when DUPLEX is selected on the MODE Control. The output from the RF port of MXR1201 is attenuated to -30 dBm for the Output Amplifier by R1209, R1210, R1213, and to -60 dBm for the DUPLEX Connector by R1208, R1209, R1211, R1212 and R1214.

2-4-19 RECEIVE AUDIO PC BOARD

An AGC circuit samples the AM audio level received from the 10.7 MHz Gen/Rec Module. It produces the control voltage for the AGC amplifiers in the 10.7 MHz Gen/Rec Module and supplies the comparative signal to break squelch. Either FM or AM audio, as selected by the MODE Control, passes through the squelch gate multiplexer to three low pass filters (80 kHz, 8 kHz and 250 Hz), then to filter select multiplexers.

One multiplexer selects either the 80 kHz or 8 kHz filter for signal routing. The signal then passes through a range select circuit to the meter function circuit. The range select and meter function circuits are controlled by the METER Control. The signal is then supplied to the Modulation Meter and the Digital Display.

The second multiplexer selects either the 8 kHz or 250 Hz filter output, which is fed to the audio/sinad switching circuit on the Generate Audio Module. When either SINAD or DIST is selected on the METER Control, any signal applied through the EXT MOD/SINAD Connector is switched into the audio circuit, disconnecting the internal audio signal. The selected signal is then returned to the Receive Audio Module. An AGC circuit controls the signal level and feeds into the Digital Module for frequency counting, and to the SINAD/Distortion circuit. The signal is then coupled through the meter function circuit for display on the Modulation Meter and on the Digital Display.

The DC signal from the Output Amplifier, is applied to a power monitor circuit. When the signal exceeds a threshold, the power monitor sends a signal to the operating mode circuit in the Generate Audio Module. The power monitor also applies the signal to the meter function circuit. When the METER Control is set for average power readings, the output of the meter function circuit is routed through an averaging circuit, then applied to the Modulation Meter and Digital Display; when peak power is selected, the averaging circuit is bypassed.

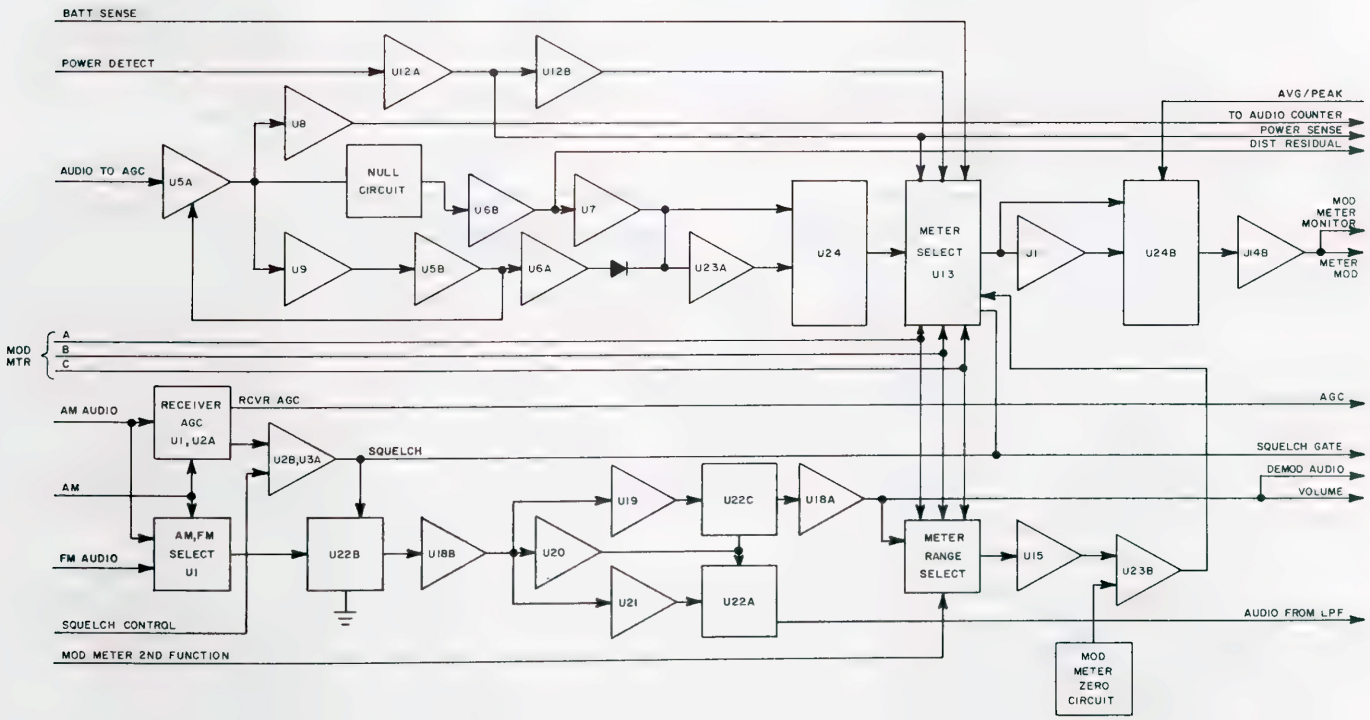


Figure 2-24 Receive Audio PC Board Block Diagram

A. SIGNAL CONTROL CIRCUIT

The AM audio signal received from the 10.7 MHz Gen/Rec Module represents the carrier amplitude for FM, carrier amplitude plus audio modulation for AM, and generator VCO amplitude plus audio modulation for SSB. This signal is applied through R3302 to op amp U3302A, whose reference level is set at approximately 1.8 VDC by R3305 and R3307. When SSB is selected, multiplexer U3301B couples R3306 and CR3301 in parallel with R3302. When AM or SSB is selected, multiplexer U3301C couples C3304 in parallel with C3301. Thus, the slew rate for U3302A is set by R3302 and C3301 for FM, R3302, C3301 and C3304 for AM, and R3302, R3306, C3301 and C3304 for SSB. This allows U3302A to respond to the carrier amplitude but not to audio modulation.

If the amplitude of the signal reaching U3302A is below the reference level, the output is a positive high, which is applied to the AGC amplifiers in the 10.7 MHz Gen/Rec Module, for maximum amplification of the RF signal. This results in an increased level to U3302A. When the signal equals the reference level, the output becomes negative, reducing the amplification by the AGC amplifiers. The stronger the received RF, the less amplification is required, thus the more negative the output of U3302A becomes. AGC amplification is now at its minimum.

CR3302 allows the negative output of U3302A to be applied to op amp U3303A, which buffers and inverts the signal. The output of U3303A goes to meter function multiplexer U3313 and to op amp U3302B. The reference voltage for U3302B is set by the SQUELCH Control. When the applied signal level exceeds the reference, U3302B supplies a high which enables multiplexer U3322B and is also routed to the Digital Module.

The FM and AM audio signals are applied through trimpots R3383 and R3379 respectively to multiplexer U3301A. The control voltage to U3301A is high when AM or SSB is selected on the MODE Control. The selected audio signal is then coupled through U3322B, when squelch is broken, to buffer U3318B. From U3318B, the signal is applied to three low pass filters.

B. LOW PASS FILTERS

The three low pass filters are identical except for R-C values. The low pass filters are two-stage R-C circuits with buffering following each stage to provide isolation. The 80 kHz filter consists of resistors R3385 through R3388, capacitors C3315 through C3318, and op amps U3319A and U3319B. The output from U3319A is applied to multiplexer U3322C. Resistors R3389 through R3392, capacitors C3319 through C3322 and op amps U3320A and U3320B form the 8 kHz filter. Its output is applied to U3322A and U3322C. The 250 Hz filter uses resistors R3393 through R3396, capacitors C3323 through C3326 and op amps U3321A and U3321B. The output from U3321A is applied to U3322A.

The signal from U3322A is routed to the Generate Audio Module. When a frequency of 409.6 Hz or less is selected on the Variable Tone Generator, U3322A switches to the 250 Hz filter. The signal from U3320 is coupled through U3322C to buffer U3318A. When FM WIDE is selected, the signal from the 80 kHz filter U3319A is selected by U3322C.

C. RANGE SELECT CIRCUIT

The audio signal from the low pass filter selected by multiplexer U3322C is buffered by op amp U3318A. From U3318A, the signal goes through the VOLUME Control to the speaker amplifier in the Generate Audio Module; through R3398 to the DEMOD Connector; through R3399 to range select multiplexer U3316 for the 2kHz/X10% range; and through a voltage divider consisting of R3400, R3401, R3404 and R3432 for additional ranges. The 6 kHz/60% range taps between R3400 and R3401 and goes directly to U3316. For 20kHz/X10%, the signal is tapped between R3401 and R3404, and goes to multiplexer U3324C. The 6kHz/X10% range taps between R33104 and R33132, and also goes to U3324C. U3324C normally couples the 20kHz/X10% level to U3316; however, when the 6kHz/X10% position is selected on the METER Control, a corresponding high command signal enables U3324C to select the 6kHz/X10% level.

The output of U3316 is coupled through buffer U3314A to a peak detector consisting of dual op amp U3315A and U3315B and associated components. The output from U3315B is a negative DC voltage equal to the peak voltage of the selected test signal, which is applied to the inverting side of op amp U3323B.

U3310, R3368 thru R3371 and R3421 thru R3424 make up a selectable voltage divider for zero reference levels during modulation measurements. U3310 selects one of four pots (R3368 thru R3371) to supply the voltage divider (R3421 thru R3424). U3317 selects the appropriate voltage for the desired modulation range. The selected level is then applied to the non-inverting input of U3323B. The output of U3323B, then, is a positive DC level proportioned, at selected ratios, to the audio signal level received at the Receive Audio Module.

D. AGC CIRCUIT

The signal from the audio/SINAD switching circuit in the Generate Audio Module is AC coupled by C3329, through opto isolator U3304 to op amp U3305A. The output of U3305A goes three places: to the sinad/distortion circuit; to op amp U3308 where it is amplified, inverted and routed to the audio counter in the Digital Module; and through C3310 to op amp U3309A.

Op amps U3309A and U3309B, with associated components, form a peak detector. The signal is applied to the inverting input of U3309A. CR3307 couples the positive component to the non-inverting input of U3309B, and CR3308 couples the negative component to the inverting input. The output from U3309B is a positive DC voltage equal to the peak voltage of the input signal.

R3326 applies -12 VDC to the inverting input of op amp U3358, whose positive output is applied to the sinad/distortion circuit and to the LED in opto-isolator U3304. As the LED increases in brilliance, the resistance in U3304 decreases, decreasing attenuation of the test signal, and resulting in greater gain through U3305A. The positive DC level from U3309B is summed with the -12 VDC at R3326, reducing the negative DC level applied to U3305B. U3305B output decreases, reducing the brilliance of the LED in U3304, which in turn increases its resistance, ultimately decreasing the gain at U3305A. C3305 establishes the slew rate of U3305B, while CR3306 limits its output to 0.6 VDC in the event the test signal level exceeds the AGC controllable level.

E. SINAD/DISTORTION CIRCUIT

The signal received from op amp U3305A passes through an RC notch filter consisting of C3306, C3307, C3327, C3328, R3317, R3319, R3321, R3322, R3323, trimpots R3318 and R3320, and buffer op amp U3306. The filter is tuned to reject only a frequency of 1000 Hz (±1 Hz at -50 dB). From U3306B, the signal is routed to the Oscilloscope for video presentation, and to a peak detector for meter display. The peak detector consists of op amps U3307A and U3307B and associated components. The signal enters the inverting input of U3307A. The positive component of its output is coupled through CR3310 to the non-inverting input U3307A and the negative component is coupled through CR3311 to the inverting input. The output of U3307B, a positive DC voltage proportional to the signal level from the notch filter, is calibrated by trimpot R3350. It is then applied to the low-enabled input of multiplexer U3324A and through op amp U3323A for input of U3324A. From U3324A, the signal is applied to multiplexer U3313.

The input to the sinad/distortion circuit from op amp U3305A is applied to the non-inverting input of comparator op amp U3306A, whose reference voltage is supplied through voltage divider resistors R3342 and R3343. If the test signal level at opto-isolator U3304 is insufficient to reduce the output of U3305B to approximately 9 volts or less, U3306A combines a high positive DC level with the output of the peak detector to peg the meter.

F. POWER MONITOR

The DC voltage from the power detector in the Output Amplifier is applied to op amp U3312. When no signal is present from the Output Amplifier, R3345 applies a negative bias to U3312B. The negative reference voltage from R3355 is applied to the inverting input of U3312B, with trimpot R3354 used to calibrate the hysteresis. CR3313 limits the output to a positive level. The output from U3312B is fed the operating mode circuit in the Generate Audio Module, and the power monitoring circuits in the Receive Audio Module. R3360, R3361 and trimpot R3362 furnish the 150W power range to multiplexer U3313. For the 15W power range, the signal is amplified by op amp U3312A, then is divided by R3366, R3367 and trimpot R3365, and applied to U3313.

G. METER FUNCTION CIRCUIT

All signals displayed on the Modulation Meter are routed to multiplexer U3313. The output of U3313 is then applied directly to the low-enabled pin of multiplexer U3324B and through an averaging circuit, consisting of op amp U3311 and associated components, to the high-enabled point of U3324B. From U3324B, the signal is buffered by op amp U3314B, then goes to the Modulation Meter and to the DVM I/O PC Board.

2-4-20 ANALYZER RF MODULE

The IF signal received from the IF module passes through a bandpass filter, is mixed with the output of a sweep oscillator, and is again filtered to 22.3 MHz. Between sweeps, the oscillator output is mixed with the output frequency of the Low Loop Module, and the difference frequency is phase locked to a 1 MHz reference from the Frequency Standard. This establishes a center frequency for the sweep which changes according to the Low Loop Frequency. The sweep control voltage then causes the oscillator to sweep from below to above its center frequency. An onboard subregulator circuit provides +11 V, -11 V and +6.9 V.

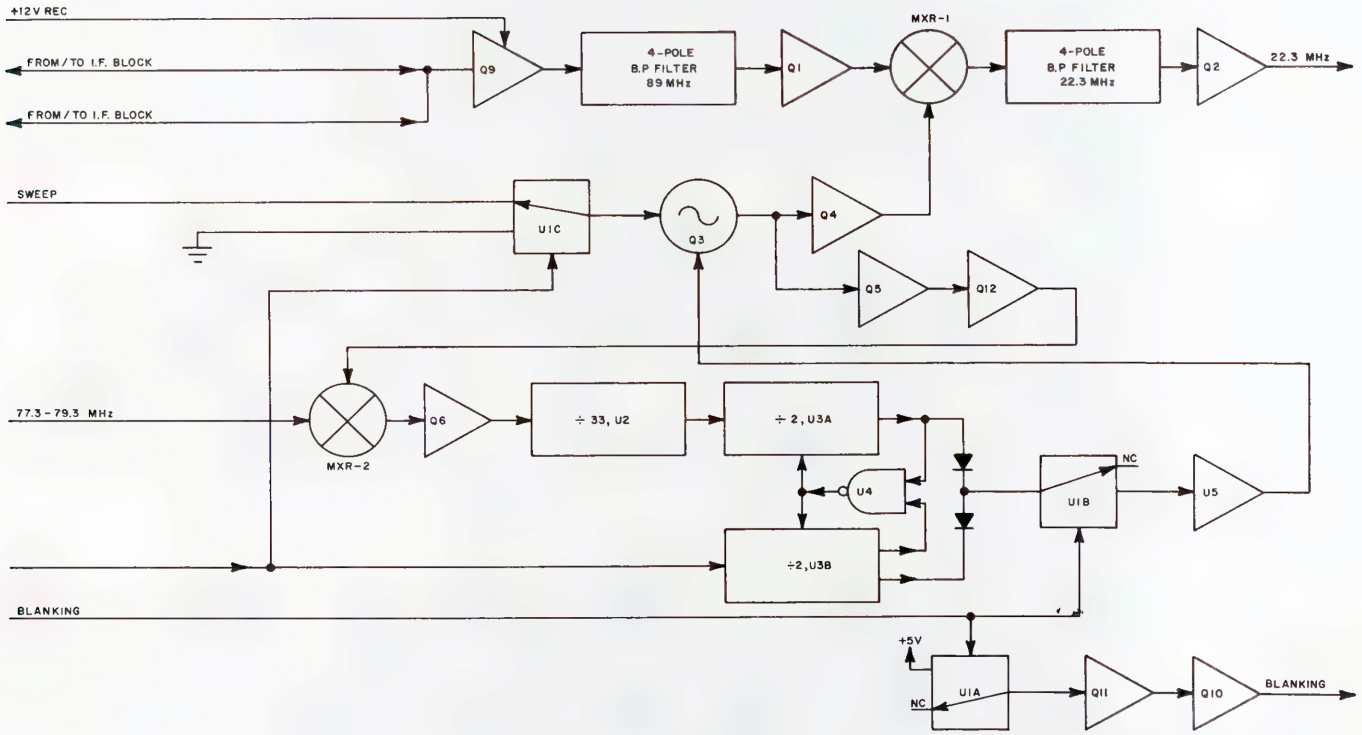


Figure 2-25 Analyzer RF Module Block Diagram

A. SUBREGULATOR CIRCUIT

The +11V subregulator consists of emitter-follower Q407, op amp U406, +6.9 V reference zener diode CR406, and a voltage divider using R441, R442 and trimpot R443 to sample the collector voltage of Q407 for comparison to the reference.

The -11V subregulator, which is similar to the +11V subregulator, consists of op amp U407, emitter-follower Q408 and a voltage divider using R439, R440 and trimpot R451. U407 uses +11 V as a reference, and the supply is -12V.

Zener diode CR401 and resistor R410 reduce the regulated +11V to +6.9V for the sweep oscillator and phase-lock circuits. Zener diode CR407 and resistor R463 reduce the +12V supply to +5V.

B. SWEEP OSCILLATOR CIRCUIT

FET Q403 is tuned by variable inductor L415 and varactor CR402 to oscillate at a center frequency of 110.3 to 112.3 MHz. The phase lock circuit control voltage applied to CR402 varies the center frequency according to the Low Loop output frequency when an analyzer blanking signal is applied. When the blanking signal is removed, multiplexer U401C applies the sweep control voltage to the tuning circuit. This voltage, which is a ramp starting negative and progressing to equally positive, pulls the frequency below center, then drives it equally above center. The next blanking signal opens the sweep control line and snaps the oscillator back to center frequency. The output level of Q403 is controlled by CR403. The signal is then filtered by L416, C423 and R421, coupled through C424 and C430 to buffers Q404 and Q405 respectively. From Q404, the signal is applied to IF Mixer MXR401; from Q405, the signal is further buffered by Q412, then applied to MXR402 in the phase/frequency comparator circuit.

C. PHASE/FREQUENCY COMPARATOR CIRCUIT

MXR402 mixes the output of the sweep oscillator with the 79.3 to 77.3 MHz output from the Low Loop. A low pass filter consisting of L418, L419, C434, C435 and C436 then passes the difference frequency to a tuned amplifier, Q406. A tank circuit consisting of L421 and C450, tunes the collector at Q406 to 33 MHz, which is the difference between the sweep oscillator center frequency of 112.3 to 110.3 MHz and the Low Loop frequency of 79.3 to 77.3 MHz. Prescaler U402 is programmed to divide by 33, producing a 1 MHz output. The 1 MHz output from prescaler U402 clocks flip-flop U403A and the 1 MHz reference clocks U403B. The corresponding Q outputs of the flip-flops are connected to pins 9 and 10 of NAND gate U404C, with the gate output from pin 8 applied to reset both flip-flops. The Q output of U403A charges capacitor C443 through diode CR404. The $\overline{Q}$ output from U403B discharges C443 through CR405. Thus, if the two input frequencies are in phase, the charge on capacitor C443 stays constant. However, if the inputs are not in phase, the charge on C443 is a DC correction voltage to pin 4 of multiplexer U401B. During analyzer blanking, multiplexer U401B couples the voltage level at C443 to op amp U405. U405, C444 and associated components form a sample-and-hold integrator circuit for tuning the center frequency of the oscillator. During blanking, the only tuning voltage is from U405, which is applied to varactor CR402. During sweep, U405 receives no input from the phase comparator, so C444 stores and holds the previous level. This allows U405 to continue, during the sweep, to furnish the same voltage as during the preceding blanking period, causing CR402 to hold this level as the center frequency level while the sweep voltage varies the frequency during the sweep period. During the next blanking period, U405 resets the center frequency control voltage and returns the oscillator to that frequency, and the charge level of C444 is adjusted accordingly for the next sweep.

D. IF MIXER CIRCUIT

In the generate mode, the 89 MHz signal from the IF Module enters at J406 and is attenuated by R454 to prevent overdriving the analyzer display. In the receive mode, +12V from the Generate Audio Module turns on Q409, which allows the 83-95 MHz signal to bypass R454. In either mode, the signal is then coupled to a 4-pole, 12 MHz bandpass filter, consisting of FL401 thru FL404 and associated components. The signal is then amplified by Q401, and mixed with the sweep oscillator signal in MXR401. A 22.3 MHz IF bandpass filter, consisting of FL405 thru FL408 and associated components, then passes only the 22.3 MHz signal. From the 22.3 MHz IF bandpass filter, the signal is amplified by Q402, then coupled to the Analyzer IF Module through J401.

E. OSCILLATOR BLANKING CIRCUIT

Power for the 33 MHz oscillator in the Analyzer IF Module is supplied through Q410 for control purposes. When the analyzer blanking signal is applied at pin 12 of J402, it enables multiplexer U401A, applying +5V to Q411. This turns on Q411, which pulls down on the base of Q410, shutting off the oscillator power.

2-4-21 ANALYZER IF MODULE

The Analyzer IF Module mixes the 22.3 MHz signal from the Analyzer RF Module with 33 MHz from a local oscillator to produce a 10.7 MHz IF. The signal is then filtered to a 3 kHz or 300 Hz bandwidth for narrow dispersion selections before being mixed with a 9.5 MHz signal from a second local oscillator. A low pass filter then passes the 1.2 MHz difference frequency for amplification which is applied to the Analyzer Log Amp Module.

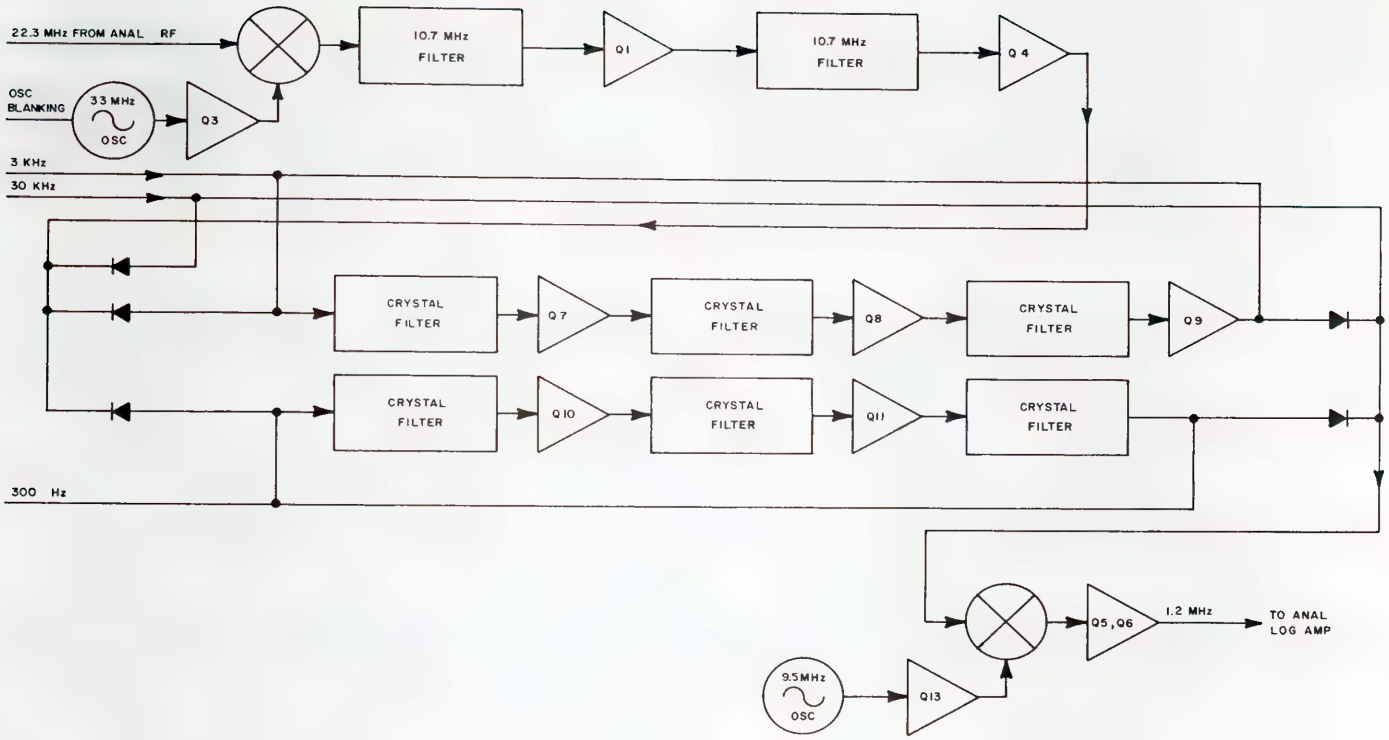


Figure 2-26 Analyzer IF Module Block Diagram

A. 33 MHz OSCILLATOR

The 33 MHz oscillator contains Q502, 33 MHz crystal Y501 and associated components. +12 volts from Q410 in the Analyzer RF Module is applied to the 33 MHz oscillator. As Y501 oscillates at its resonant frequency, the signal is amplified by Q502. The pulses produced at the emitter of Q502 are applied to the base of Q503. Q503 then buffers the 33 MHz for MXR501. When blanking occurs, the oscillator power is interrupted, which disables the 33 MHz oscillator.

B. 10.7 MHz MIXER CIRCUIT

A low pass filter consisting of C575, C579, and L517, filters any induced RF from the VCO in the Analyzer RF Module from the 22.3 MHz IF. MXR501 then combines the 22.3 MHz IF with the 33 MHz level oscillator output producing the 10.7 MHz IF. The 10.7 MHz IF then passes through a 4-pole, 600 kHz bandpass filter consisting of FL501 thru FL504, is amplified by Q501, then filtered by a second 4-pole, 600 kHz bandpass filter consisting of FL505 thru FL508.

C. BANDWIDTH FILTER CIRCUIT

When a dispersion range of 50 kHz or greater per division is selected on the HORIZONTAL Sweep Control, +12 V is applied to forward bias CR504 and CR507, coupling the 10.7 MHz IF from Q504 directly to MXR502. CR505, CR506, CR508 and CR509 are reverse biased to isolate the 300 Hz and 3 kHz filters. 30 kHz bandwidth filtering for these dispersion selections is in the Analyzer Log Amplifier Module.

For dispersion selections of 5 kHz, 10 kHz and 20 kHz per division, +12 V is applied to forward bias CR506 and CR508 and reverse bias CR504, CR505, CR507 and CR509, directing the signal through the 3 kHz filter. The three-stage filter circuit contains three crystals, YFL501, YFL502 and YFL503, each with two trimcaps for signal amplitude and shape, followed by amplifying transistors, Q507, Q508 and Q509, respectively. Trimpot R543 adjusts the total gain of the three transistors to compensate for filter losses.

When the HORIZONTAL Sweep Control is in the 1 kHz or 2 kHz per division dispersion position, +12 V forward biases CR505 and CR509 and reverse biases CR504, CR506, CR507 and CR508 to direct the signal through the 300 Hz filter. This circuit contains six matched crystals, YFL504 through YFL509, in three paired stages. A fixed amplifier, using Q510, follows the first stage and an adjustable amplifier, using Q511 and trimpot R559, follows the second stage. Total gain from the amplifiers is adjusted to compensate for filter losses.

D. 9.5 MHz OSCILLATOR CIRCUIT

Y511 is a 9.5 MHz crystal which controls the base voltage of Q512. The signal produced, is amplified by Q513 and coupled through C553 to MXR502.

E. 1.2 MHz MIXER CIRCUIT

MXR502 combines the 10.7 MHz IF signal with the 9.5 MHz signal. A low pass filter consisting of C536, C544 and L512 passes only the 1.2 MHz difference frequency. The signal is then amplified by Q505 and Q506 to 30 dB above the level received at the Antenna or T/R Jack, and coupled through C522 and J503 to the Analyzer Log Amp Module.

2-4-22 ANALYZER LOG AMPLIFIER MODULE

The logarithmic amplifier (log amp) converts the nonlinear amplitude of the swept IF signal into a linear output for the analyzer vertical drive. In addition to containing the log amplifier, this module also contains the 30 kHz bandpass filter due to space limitations in the Analyzer IF Module.

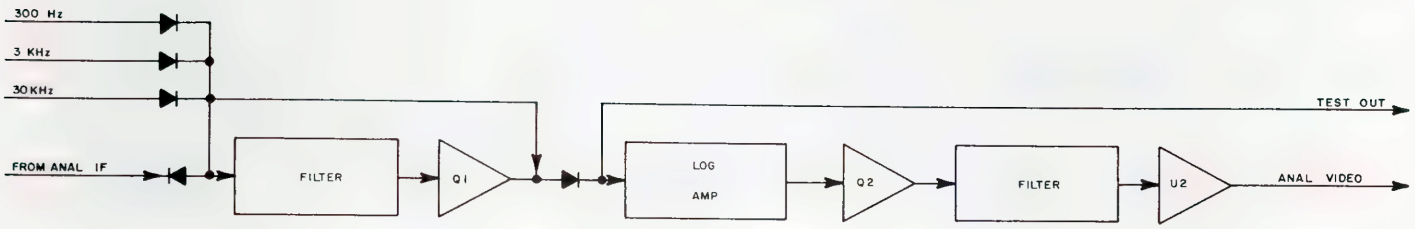


Figure 2-27 Analyzer Log Amp Block Diagram

A. 30 kHz BANDPASS FILTER CIRCUIT

When any analyzer dispersion range is selected on the HORIZONTAL Sweep Control, +12 V forward biases CR804 and CR807 and reverse biases CR805 and CR806. This directs the 1.2 MHz IF through a 6-pole, 30 kHz bandpass filter, consisting of FL801 thru FL806, and an amplifier to restore filter loss. Trimpot R809 calibrates the gain produced by Q801. J803 is a test port for the IF signal, which should be 10 dB above the received signal level.

B. LOG AMP CIRCUIT

The log amp circuit contains log amp IC U801, transformer T801 and two tuned amplifier stages. The 1.2 MHz IF is applied directly to U801, through trimpot R812, to the base of Q804 in the first amplifier stage. Trimpot R818 sets the gain of Q804 which, in turn, drives Q803. Q803 is tuned to 1.2 MHz by L810 and C834, with its output level limited by CR809 and CR810 to one diode gap above and below ground. This level is applied to U801 and to the base of Q805 in the second amplifier stage. The second stage, consisting of Q805, Q806 and associated components, is identical to the first stage, and is applied only to U801. All three trimpots in this circuit interact with the trimpots in the analyzer vertical drive circuit.

The output of U801 consists of two summations, linearly representing the logarithmic inputs. Each summation contains two outputs, Y, $\overline{Y}$ and Z, $\overline{Z}$ which are equal in amplitude but opposite in polarity. The Y and Z outputs are applied to one terminal of the primary of T801 and the $\overline{Y}$ and $\overline{Z}$ outputs are applied to the other terminal. T801 blocks the DC potential, couples the linearized output to the analyzer vertical drive circuit, and isolates the drive circuit from the log amp circuit.

C. ANALYZER VERTICAL DRIVE CIRCUIT

Emitter-follower Q802 is biased by +5.1 V, which passes through the secondary winding of T801. This allows the output from the log amp, U801, to be coupled with the bias for Q802. The gain of Q802 is set by R821 and thermistor TR801. L808 and C824 tune the amplifier to 1.2 MHz. DC blocking capacitor C825 couples the RF signal to a rectifier/detector circuit.

+5.1 VDC is applied to the rectifier/detector circuit through a voltage divider consisting of R828, CR815 and trimpot R832 to adjust the base line level. The positive component of the signal pulse passes through AM detector CR814 to charge C828, which is discharged through R833 and trimpots R830 and R832. The circuit is tuned with L809, C826 and C827.

The reference level for op amp U802B is calibrated with R829 and trimpot R831. The output level from the rectifier/detector circuit, which is calibrated by R830, is applied to U802B for amplification. From U802B, the signal is routed through J801, pin 1 to the Scope Control Module.

All trimpots in the analyzer vertical drive and log amp circuits are interactive.

2-4-23 SCOPE POWER AND CONTROL ASSEMBLY

2-4-23-1 SCOPE CONTROL PC BOARD

The Oscilloscope Control Board controls the sweep rate and the horizontal and vertical deflection for the Oscilloscope and Spectrum Analyzer functions. For the Oscilloscope function, it contains the sweep trigger and the vertical drive circuits. The analyzer sweep circuit also provides calibration adjustments for centering and dispersion. All mode and range selections are achieved by two ganged, rotary switches mounted on the Oscilloscope Control Board and extending through the Front Panel.

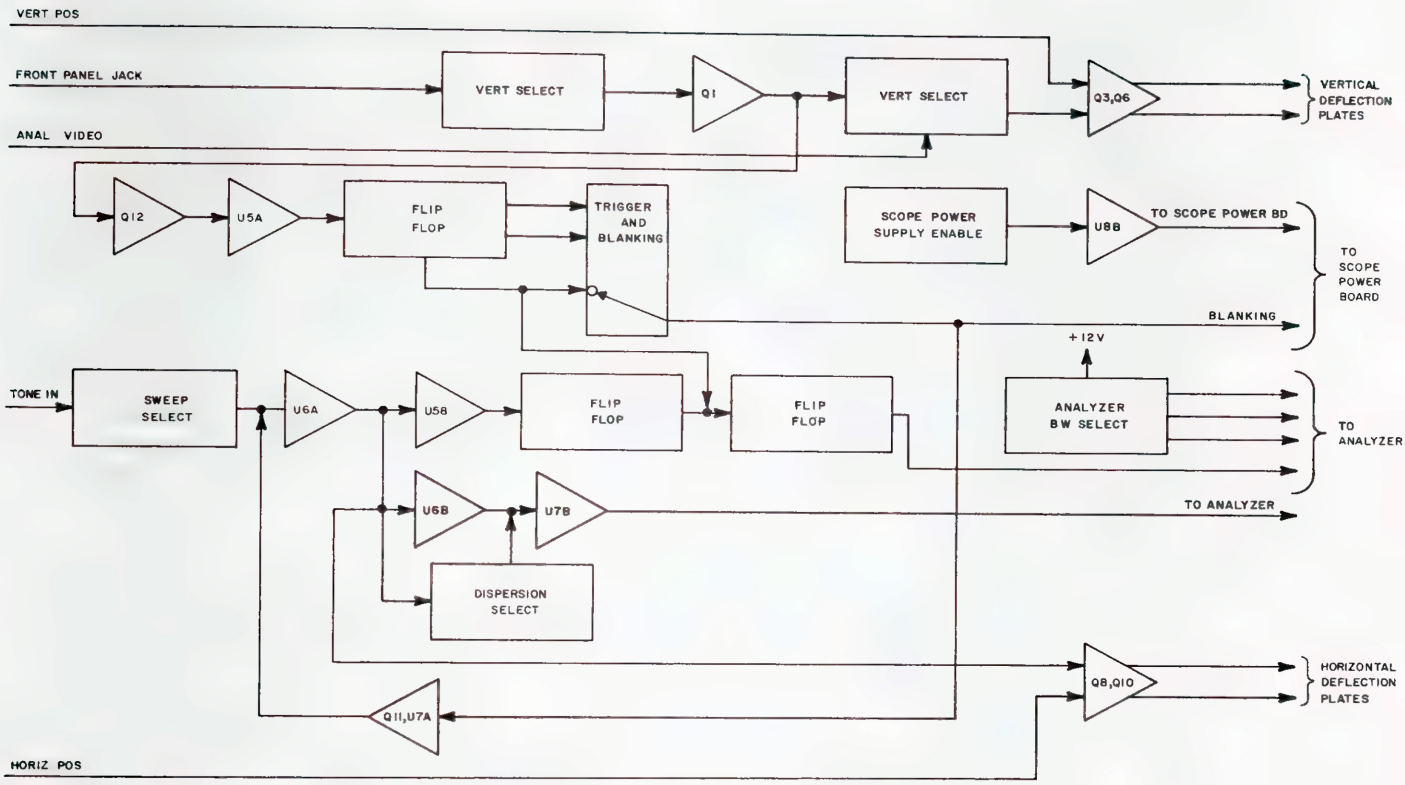


Figure 2-28 Scope Control PC Board Block Diagram

A. SCOPE ENABLE CIRCUIT

Op amp U208B functions as a comparator to provide a high output to the Oscilloscope Power Supply Board when SW201 (VERTICAL Attenuator Selector) is in the "OFF" position. In any other position, SW201 allows +12 V to be applied to pin 6 of U208B, exceeding the reference voltage of +7 V at pin 5, which allows the Oscilloscope Power Supply to operate. In the "OFF" position, SW201 grounds the +12 V control.

B. HORIZONTAL DRIVE CIRCUIT

The sweep rate is set by a switch, consisting of Q211 and op amp U207A, a ramp generator using a constant current source, Q202 and associated components, and one capacitor, either C218, C219, C220, C221 or C228 as selected by SW202. When Q211 is turned on, op amp U207A pulls the ramp voltage to -0.5 V; when it is turned off, the ramp voltage increases at the rate determined by the selected capacitor and the constant current drawn through Q208. Buffer U206A applies this ramp signal to the horizontal deflection circuit, the analyzer sweep divider circuit, and op amp U205B. U205B is

configured as a comparator, which is calibrated by R244, R245 and R293 to trigger when the output of U206A reaches +0.5 V. When U205B sets flip-flop U203B, the high Q output performs four functions. First, it supplies the reset trigger for U209A to reset the trigger function. Second, it charges C217 in the free-run timer until the timer resets U203B, pulling Q low. Third, it supplies a high through multiplexer U204 to blank the Oscilloscope and, simultaneously, turns on Q211, terminating the sweep. When the free-run timer resets U203B, blanking signal ends and Q211 turns off, allowing the next sweep to commence. Fourth, it clocks flip-flop U203A to blank the Spectrum Analyzer until its blanking timer, consisting of R297 and C233, resets U203A. As R248 (Sweep Vernier Control) is rotated CCW the base voltage of Q202 increases. This increase in base voltage decreases the current flow through Q202, slowing the sweep rate. R248 is bypassed by U202B when in analyzer operation.

When SW202 (Horizontal Sweep Selector) is in the "TONE" position, Q202 is coupled to R250 to provide a constant current. Any tone applied to the modulator circuit of the Generate Audio Module is then applied to the sweep generator circuit and its amplitude generates the horizontal component of the trace. SW202 also switches U204 to the Tone mode, which applies -7 V to the oscilloscope blanking circuit in the Oscilloscope Power Supply to prevent blanking, and to the base of Q211, keeping it turned off.

C. HORIZONTAL DEFLECTION CIRCUIT

The horizontal deflection circuit consists of a buffer amplifier and a differential amplifier. The sweep signal from buffer U206A is applied to buffer U208A. R271 allows calibrating the gain of U208A so the trace will sweep exactly the width of the screen. The output of U208A biases Q209 in the differential amplifier. The horizontal position reference signal, as established with the front panel HORIZ POS Control, is applied to the base of Q208. Q210 and associated components form a constant current source drawing equally on Q208 and Q209. As the bias voltages differ between Q208 and Q209, the current flow through them varies inversely, causing the horizontal deflection plate voltages to vary proportionately to the difference in the bias voltages.

When SW202 is not in a mS/DIV position (Oscilloscope operation), U202C routes the horizontal position control signal through a voltage divider to attenuate the effect of the control.

D. INPUT ATTENUATION CIRCUIT

An external signal applied through the SCOPE Connector, routed through the AC-DC Switch, is applied to pin C of SW201. Demodulated audio signals from the Receive Audio Module are applied through R201 to pin B and to a voltage divider consisting of R202 and R203. The signal level is divided by four through the voltage divider and applied to pin A of SW201. Depending upon the Front Panel selection of SW201, the signal applied at pin A, B or C is coupled to the appropriate input attenuator at pin D, E or F.

The ÷1 circuit connects pins C and D of SW201, providing no attenuation. C202 and R281 provide input impedance for the Oscilloscope. The X10 circuit consists of C203, C204, R205 and R206, and connects pins C and E of SW201. The X100 and X1000 is a ladder circuit consisting of C201, C205, C206, R207, R208 and R209. The circuit connects pin K to pin M to divide by 100, and pin L to pin M to divide by 1000. All attenuators provide approximately 17 pF capacitance and 1 M ohm resistance for Oscilloscope input impedance.

The distortion residual from the Receive Audio Module is applied through a 10:1 voltage divider consisting of R210 and R211 to pin N of SW201.

E. OSCILLOSCOPE VERTICAL DRIVE CIRCUIT

From SW201 pin M, the selected signal is passed across a limiter consisting of CR201 and CR202, then applied to the gate of FET Q201A. Q201 is a dual FET manufactured on the same substrate. Q201A is a current follower while Q201B is a constant current source calibrated by R215. As the input signal amplitude varies, changing the current flow through Q201A accordingly, the current flow through R216 and R217 varies as to maintain a constant current through Q201B. The signal which is received from the attenuators in the form of voltage is converted to current through R216 and R217 by Q201A, Q201B and related components. The signal is attenuated approximately 4 dB, and applied to the vertical deflection preamp, U201A. The gain of U201A calibrated by R221, is approximately +24 dB, making the net gain of the circuit approximately +20 dB.

F. VERTICAL DEFLECTION CIRCUIT

Vertical deflection is accomplished with a differential amplifier consisting of discrete transistors Q203 through Q207, and related components. A vertical position reference signal, between -12 VDC and +12 VDC as established with the Front Panel VERT POS Control, is applied to the base of Q206. SW202 (HORIZONTAL Sweep Selector) applies a signal from the vertical drive circuit of either the Oscilloscope or Spectrum Analyzer to the base of Q205. Q207 and associated components form a constant current source drawing current through the two amplifiers Q203/Q205 and Q204/Q206. As the bias voltages differ between Q205 and Q206, the current flow through them varies inversely, causing the vertical deflection plate voltages to vary proportionately to the difference in the bias voltages.

When SW202 is not in a mS/DIV position, switch U202A routes the vertical position control signal through a voltage divider to attenuate the effect of the control.

G. SCOPE TRIGGER CIRCUIT

The signal from the oscilloscope drive circuit is buffered by Q212, with C231 and C232 removing any DC component, leaving only the AC components referenced to ground potential. This signal is applied to pin 3 of op amp U205A. U205A functions as a Schmitt trigger and provides a high output for the positive portions of the signal. U205A clocks D-type flip-flop U209A with the leading edge of the pulse, providing a positive only, non-selectable trigger. The high $\overline{Q}$ output from U209A charges C216 and switches multiplexer U204 to couple the $\overline{Q}$ output to its output at pin 3. This turns off Q211 and allows the sweep to commence. When the sweep is finished and U205B sets U203B, the high Q from U203B resets U209B. The next trigger pulse from U205A again sets U409A, and the cycle repeats. C216 holds U204 in the trigger mode for at least one-half second to provide the ability to trigger on low frequencies or partial waveforms. If no trigger is received during this period, U204 will revert to the free-run mode.

H. ANALYZER SWEEP CIRCUIT

The output from U206A to the analyzer sweep circuit is amplified by op amp U206B and U207B to an output from -7 V to +7 VDC with SW202 in the 1 MHz/DIV position. R260 allows calibration of this output. For other dispersion positions, SW202 provides a ground path through one of three voltage dividers for U206B, and through one of two voltage dividers for U207B. R298 provides a DC offset voltage to be summed with the sweep signal before routing it to the Analyzer RF Module.

2-4-23-2 SCOPE POWER SUPPLY PC BOARD

The only power required by the CRT Power PC Board is +12 VDC, supplied through the Oscilloscope Control Board. An oscillator, controlled by a scope enable command, produces timing squarewaves to power the transformer circuit. The transformer supplies all voltages required by the CRT.

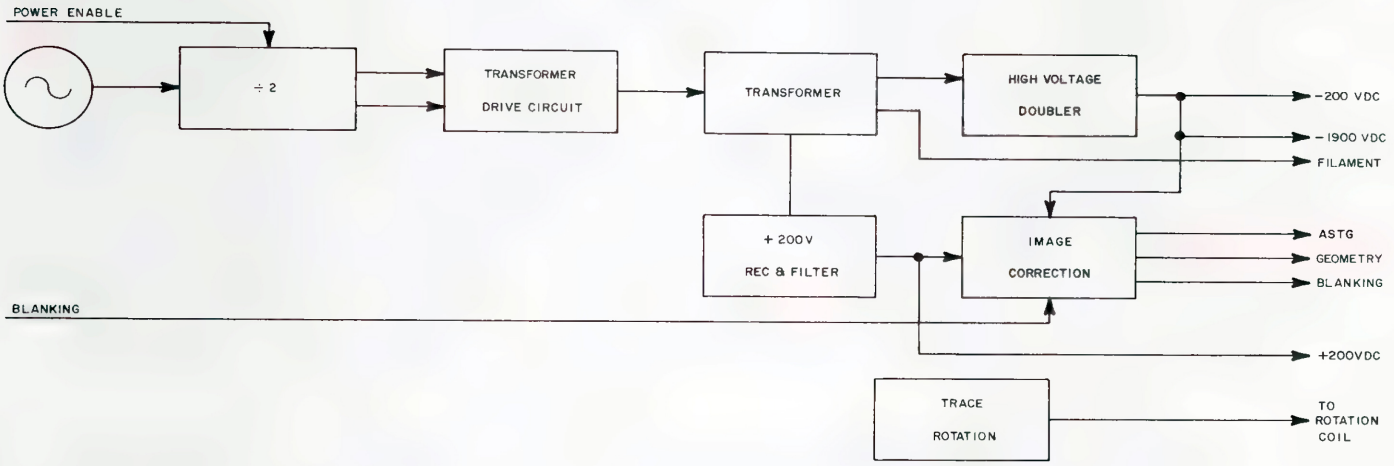


Figure 2-29 Scope Power Supply PC Board Block Diagram

A. OSCILLATOR OUTPUT CIRCUIT

A 90 kHz oscillator is formed by NOR gates U301A and U301B, which clock J-K flip-flops U302A and U302B simultaneously. With +12 VDC applied to the J and K inputs of U302A, the Q and $\overline{Q}$ outputs alternate between high and low. Q of U302A provides the J and K inputs to U302B. Since U302B changes state only when J and K are high (U302A Q is high), its frequency is half that of U302A. Only with U302A Q and U302B $\overline{Q}$ both low, NOR gate U301D provides a high to the transformer circuit. Likewise, when U302A $\overline{Q}$ and U302B Q are both low, U301C provides a high to the transformer circuit.

When the VERTICAL Attenuator Selector on the Front Panel is in the "OFF" position, the Oscilloscope Control Board supplies a high command to the reset terminal, pin 4, of U302A to inhibit the oscillator circuit output to the Transformer circuit.

B. TRANSFORMER CIRCUIT

Power is supplied through a filter consisting of C304, C305 and torroid L301 to the center tap of the primary winding of tranformer T301. R325 normally grounds the gate of FET Q305. When U301D output goes high, Q301 applies power to the gate of Q305. Q305 grounds one end of the primary winding. Similarly, U301C controls Q303, which supplies the gate voltage to FET Q306. When Q303 is off, R324 grounds the gate of Q306. Q306 grounds the opposite end of the primary winding. The effective power applied to the primary winding of T301 is then 24 VAC.

The high voltage secondary winding produces 1000 VAC. This is rectified and doubled by CR301 and CR302, C306 and C307. The resulting -2000 VDC is then applied to the CRT grid and to a voltage divider consisting of fixed resistors R307, R311, R313, R314 and R315 and potentiometers, R308 and R312. R308 provides -1900 VDC for the cathode (intensity) and R312 provides -1500 V for the focus of the beam. The low voltage secondary winding provides 6.3 VAC for the CRT filament. This voltage is also a DC offset to the -1900 VDC.

The middle voltage secondary winding output is rectified by CR303 through CR306, and filtered by R310 and C309 through C312 to supply +200 VDC to the image correction circuit, and to the Oscilloscope Control Board for horizontal and vertical deflection.

C. IMAGE CORRECTION CIRCUIT

The +200 VDC from the transformer circuit is reduced to approximately +100 VDC by R316 for calibration of CRT astigmatism (vertical component of the beam). Q308 is an emitter-follower which furnishes approximately +100 VDC for the CRT geometry (horizontal component of the beam). R317 calibrates the base voltage of Q308.

D. DISPLAY BLANKING CIRCUIT

While the display trace is displayed on the CRT screen, Q309 applies the display blanking to the geometry supply from Q308. When the trace is not displayed (i.e., during retrace), the beam is shifted off the screen without suppressing its intensity. During the blanking command from the Oscillsocope Control Board, Q307 conducts, pulling down on the emitter of Q309 and simultaneously applying voltage to its base. This turns off Q309, allowing the voltage on the display blanking and the base of Q309 to drop to approximately +10.8 VDC. When the blanking command is removed, Q307 turns off, allowing the display blanking line to float. Q307 simultaneously removes the base voltage to Q309, allowing it to conduct. This snaps the display blanking line back to its original level and returns the beam to the CRT screen.

E. ROTATION CIRCUIT

R322 applies a 0-12 VDC level to the rotation coil of the CRT to align the trace with the horizontal axis of the screen graticule. If the range of R322 is insufficient to fully align the trace, rotation of connector P/J301 by 180° will reverse the polarity of the coil. The trace can then be aligned using R322.

2-4-24 KEYBOARD

The keyboard is a 4 x 6 Matrix PC Board with 24 independent momentary pushbutton switches. Two buses (4-bit and 6-bit) connect the CPU to the keyboard. The CPU forces all 4 lines of the 4-bit bus low simultaneously. When a key is depressed, an interrupt is generated which causes the CPU to strobe the 4-bit bus lines. This low will be detected by one of the lines on the 6-bit bus, to determine which key is depressed.

2-4-25 DISPLAY PC BOARD

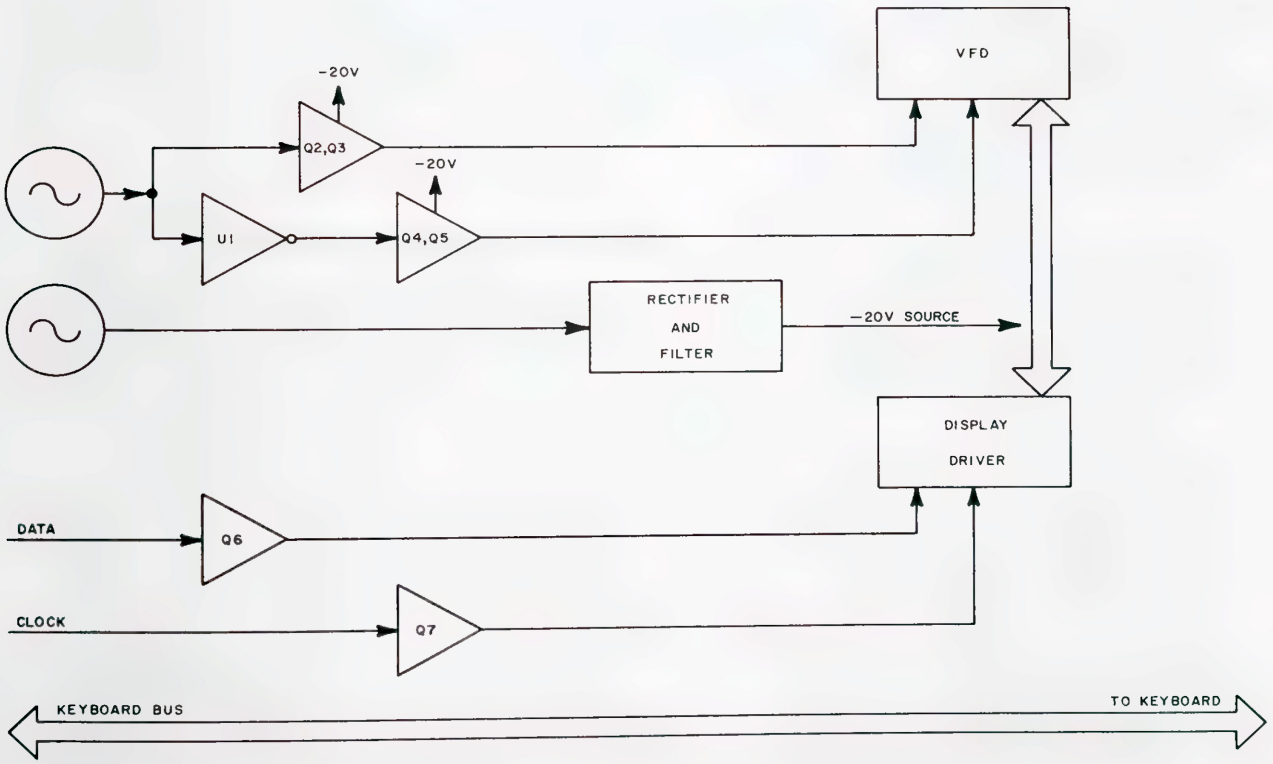


Figure 2-30 Display PC Board Block Diagram

A 16-character vacuum fluorescent display (VFD), DS1401, and its driver, U1403, are installed on the Display Board, which is mounted on the Front Panel. The Keyboard is also assembled with the Display Board.

Power to operate the VFD and the driver chip is furnished by an onboard power supply which converts -12 VDC to -3 VDC and -20 VDC. An oscillator switches these two voltages across the two power pins of DS1401 to produce approximately 30 VAC. Timer U1402 is connected between -12 VDC and ground. R1411, R1412 and C1409 establish the RC time constant for a stable operation, producing -12 V pulses. C1410 couples the pulses to -12 VDC supplied through CR1401, to produce -12 V pulses riding on -12 VDC. C1411 filters this supply to approximately -20 VDC. R1404, R1405, C1405 and inverters U1401E and U1401F form an oscillator which drives switching transistors Q1402 and Q1403 through inverter U1401A and transistors Q1404 and Q1405 through U1401C and U1401D. Q1401 regulates the -20 VDC to -3 VDC, which is applied to the collectors of Q1402 and Q1404, with -20 VDC being applied to the collectors of Q1403 and Q1405. As the inverter switches the transistors on and off, -3 VDC and -20 VDC (minus losses) are alternately switched between pins 1 and 37 of DS1401. This produces the effect of -15 VAC to DS1401.

A clock signal from the CPU is supplied to U1403 through level converting transistor Q1407. Data is furnished through level converting transistor Q1406. When U1403 is clocked, it shifts existing data one place to the left and presents the new data in the just vacated right hand position.

2-4-26 FUNCTION SWITCH PC BOARD

The Function Switch PC Board contains the front panel meters, squelch and volume controls, tone select and level controls, and four rotary switches for selecting meter function, mode, freq error range, and modulation. All switching lines are routed to the Interface PC Board, except the modulation lines, which are routed first to the motherboard, then to the appropriate modules.

SECTION 3 - PEFORMANCE EVALUATION

3-1 GENERAL

This section contains step-by-step test procedures for assessing the performance of the FM/AM-1200. These procedures should be relied upon as the first step in the troubleshooting/maintenance process, when the operating condition of the set is in question. All procedures contained in this section are performed using the FM/AM-1200 front and rear panel controls, indicators and connectors and does not require the removal of the exterior case.

The test procedures contain several common headings which are defined below:

3-2-1	Test procedure number.
PERFORMANCE EVALUATION:	Name of test procedure to be performed.
SPECIAL ACCESSORY EQUIPMENT REQ'D:	List of any special accessory test equipment required to complete the test procedure.
INITIAL CONTROL SETTINGS:	Initial FM/AM-1200 front and rear panel control settings required to begin the test procedure. (Refer to Figure 1-2 on foldout page in Section 1 for front and rear panel control identification.)

3-1-1 PRE-OPERATIONAL CONSIDERATIONS

For maximum benefit of all operating procedures herein, it is strongly recommended that personnel:

1. Thoroughly read and understand all steps of procedure to be performed, prior to its completion.

2. Be familiar with the circuit or unit under test so some idea is perceived as to the power, frequency and waveform to be expected at each test point. This knowledge will aid personnel in performing the test procedure in a logical and efficient manner.

3-1-2 TEST EQUIPMENT REQUIREMENTS

Appendix B at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures in this manual. Any other equipment meeting the specifications listed in the appendix, may be substituted in place of the recommended models.

NOTE

For certain procedures in this manual, the equipment listed in Appendix B may exceed the minimum required specifications.

3-1-3 CORRECTIVE MAINTENANCE PROCEDURES

The performance checks in this section will aid the operator/technician in determining whether the FM/AM-1200 is functioning properly or if a failure condition exists. A failure condition will normally be reflected as either a calibration error or a malfunction. A calibration error is defined as a measurement or reading (relating to the unit being tested) that is not within prescribed tolerance. In this condition, the set may outwardly appear to be functioning properly, despite the presence of a calibration error. A malfunction denotes a defective condition where a signal may be totally absent, grossly out of tolerance or where the unit itself (or any part thereof) is obviously not working properly.

In event a failure condition is confirmed, the technician should take appropriate corrective action to return the set to its normal operating condition.

3-2 PERFORMANCE EVALUATION

3-2-1 FREQUENCY STANDARD PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQUIRED: (See Appendix B for Test Equipment Requirements)

1 Frequency Counter or 10 MHz Frequency Standard and Oscilloscope

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	SETTING
22	PWR/OFF/BATT Switch	"PWR" Position

STEP PROCEDURE

1. Using Frequency Counter:

   a. Connect Frequency Counter to External Reference Connector (45). Verify the frequency is 10 MHz with the following tolerance:

      (1) With standard TCXO ±5 Hz
      (2) With optional TCXO (Opt 01) ±2 Hz
      (3) With optional oven oscillator (Opt 02) ±.5 Hz

2. Using external 10 MHz Frequency Standard and Oscilloscope:

   a. Connect External Reference Connector (45) to X input of Oscilloscope.

   b. Connect external Frequency Standard to Y input of Oscilloscope.

   c. Verify a Lissajous pattern is displayed on the Oscilloscope.

3-2-2 RECEIVE MODE PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQUIRED: (See Appendix B for Test Equipment Requirements)

1 Signal Generator
1 3-ft Coax Cable with BNC/BNC Connectors

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	SETTING
3	MODULATION Select Control	"FM NAR" Position
4	MODULATION Meter Control	"20 kHz/% x 10" Position
22	PWR/OFF/BATT Switch	"PWR" Position
26	HORIZONTAL Sweep Selector Control	"1 MHz/DIV" Position
35	FREQ ERROR Meter Range Selector Control	"RF 10K" Position
39	MODE Selector Control	"REC" Position
41	SQUELCH Control	Fully ccw Position

STEP PROCEDURE

1. Adjust Signal Generator to 25.50 MHz, modulated with a 1 kHz tone at 5 kHz deviation, at a level of -40 dBm output.

2. Connect Signal Generator to ANTENNA Connector (34).

3. Using Keyboard (18), select "RF 025.5000" MHz and "2nd Function - Meter". Verify the FREQ ERROR Meter (36) and VFD (37) show "0" frequency error and the Analyzer shows a -40 dBm signal level.

4. Verify modulation readings on the MODULATION Meter (1) and VFD (37) as follows:

CONTROL SETTING			FM/AM-1200 DISPLAY	
SIGNAL GENERATOR MODULATION	MODULATION SELECTOR (3)	METER RANGE SELECTOR (4)	MODULATION METER (1)	VFD (37)
5K FM	FM NAR	6	5	MD 5.000
5K FM	FM MID	6	5	MD 5.000
5K FM	FM WIDE	6	5	MD 5.000
30% AM	AM NAR	6	3	MD 3.000
30% AM	AM NORM	6	3	MD 3.000

5. Disconnect Signal Generator. Set MODULATION Select Control (3) to "FM NAR" position and adjust SQUELCH Control (41) to just silence receiver.

6. Adjust the Signal Generator for no modulation and reconnect it to the ANTENNA Connector (34).

STEP PROCEDURE

7. Select the following frequencies on the FM/AM-1200 and the Signal Generator and verify receiver sensitivity is -101 dB or greater.

255.5000 MHz	855.5000 MHz
455.5000 MHz	999.9999 MHz

8. Disconnect the Signal Generator. Select RF 151.0000 MHz on Keyboard (18) and METER Range Selector Control (4) to "WATTS - PK 15" Position.

9. Rotate SQUELCH Control (41) cw just enough to squelch the receiver.

10. Adjust RF Signal Generator for a signal of 151.0000 MHz at -90 dBm. Connect Generator to the ANTENNA Connector (34) of FM/AM-1200. Verify signal breaks squelch.

11. Decrease the Signal Generator output sufficiently to squelch the receiver, then increase the level until it just breaks squelch. Note this level. (The level should be less than -101 dBm.)

12. To verify adjacent channel rejection (ACR), reduce the signal level to squelch the receiver, then increase the level until it just breaks squelch at each of the following frequencies and bandwidths. The level noted in Step 4 must be at least 40 dB below the levels obtained in this step.

SIGNAL GENERATOR FREQUENCY (MHz)	FM/AM-1200 FREQUENCY (RF-MHz)	MODULATION SELECTOR	ACR
151.0270	151.0000	FM NAR	40 dB down
151.3000	151.0000	FM MID	40 dB down
151.3000	151.0000	FM WIDE	40 dB down

13. Disconnect Signal Generator. Set MODULATION Select Control (3) to "SSB" position, select RF 000.0010 MHz on the Keyboard (18), then rotate VOLUME Control (40) cw as required to verify a tone of approximately 1 kHz is audible from the Speaker.

14. Set the FM/AM-1200 controls as follows:

CONTROLS	INITIAL SETTINGS
3 MODULATION Select Control	"FM NAR" Position
5 VAR Tone Selector Switch	"OFF" Position
7 1 kHz Tone Selector Switch	"OFF" Position
8 1 kHz Tone Level Control	Fully ccw Position

15. Connect coax cable between ANT Connector (34) and External Reference Connector (45).

16. Verify FREQ ERROR Meter reads zero.

STEP PROCEDURE

17. Using Keyboard (18) and FREQ ERROR Range Selector Control (35) select each meter range/frequency combination in Table 3-1, in order given, and make the corresponding verifications.

FREQ ERROR Meter Range Selector Control (35) Setting	Selected Frequency	FREQ ERROR Meter (36) Indication	Tolerance
RF 10K	RF 010.0100 MHz RF 009.9900 MHz RF 009.9870 MHz	-1.00 +1.00 Pegged +	±.03% ±.03%
RF 1K	RF 009.9970 MHz RF 009.9990 MHz	Pegged + +1.00	±.03%
RF 100	RF 009.9999 MHz	+1.00	±.03%
RF 3K	RF 010.0030 MHz RF 009.9970 MHz	-3.0 +3.0	±.09% ±.09%
RF 300	RF 009.9997 MHz	+3.0	±.09%
RF 30	RF 010.0000 MHz	0	±.09%
AUDIO 300	TONE 01000.0 SINE TONE 01300.0 SINE TONE 00700.0 SINE	0 -3.0 +3.0	0 ±.09% ±.09%
AUDIO 30	TONE 01030.0 SINE TONE 00970.0 SINE	-3.0 +3.0	±.09% ±.09%
AUDIO 3	TONE 01003.0 SINE TONE 00997.0 SINE	-3.0 +3.0	±.09% ±.09%

Table 3-1 Frequency Error Meter Verification Chart

18. Remove coax cable and disconnect test equipment.

3-2-3 GENERATE MODE PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQUIRED: (See Appendix B for Test Equipment Requirements)

1 Spectrum Analyzer
1 Function Generator
1 Microwattmeter
1 Modulation Meter
1 Frequency Counter

INITIAL CONTROL SETTINGS:

	CONTROL	SETTING
3	MODULATION Select Control	"FM WIDE" Position
4	MODULATION Meter Control	"6 KHz/% x 10" Position
5	VAR Tone Selector Switch	"OFF" Position
6	VAR Tone Level Control	Fully ccw Position
7	1 kHz Tone Selector Switch	"OFF" Position
8	1 kHz Tone Level Control	Fully ccw Position
9	RF Level Attenuator Control	Fully ccw Position
10	RF Level Attenuator Vernier Control	"-30 dBm" Position
22	PWR/OFF/BATT Switch	"PWR" Position
32	GEN/LOCK Control	"Lock" Position
39	MODE Selector Control	"GEN" Position

STEP PROCEDURE

1. Connect Frequnecy Counter to T/R connector (11).

2. Using Keyboard (18), select each of the frequencies in Table 3-2 and verify frequency accuracy with the Frequency Counter.

FREQUENCY (MHz)	FREQUENCY TOLERANCE (Hz)		
	STD TCXO (.5 PPM)	OPT TCXO (.2 PPM)	OPT OVEN (.05 PPM)
000.5000	±.25	±.10	±.025
002.5000	±1.25	±.50	±.125
012.5000	±6.25	±2.50	±.625
042.5000	±21.25	±8.50	±2.125
142.5000	±71.25	±28.50	±7.125
342.5000	±171.25	±68.50	±17.125
642.5000	±321.25	±128.50	±32.125
999.9999	±500.0000	±200.00	±50.000

Table 3-2 Generate Frequency Accuracy

3. Disconnect the Frequency Counter and connect Spectrum Analyzer to T/R Connector (11). Select each of the frequencies in Table 3-2 and verify the tolerance is ±2.5 dB for the output level at -30 dBm and -110 dBm.

STEP PROCEDURE

4. Select "RF 500.0000" MHz on the Keyboard (18). Rotate the RF LEVEL Attenuator Vernier Control (10) through its entire range and verify the output level shifts at least 11 dB.

5. Disconnect Spectrum Analyzer and connect Modulation Meter to T/R Connector (11).

6. Disconnect the Modulation Meter and connect Frequency Counter to the DUPLEX Connector (14).

7. Select "FM MID" on the MODULATION Selector (3), "DUP" on the MODE Selector (39), and "RF 150.0000" on the Keyboard (18).

8. Using the Keyboard (18), select each of the following offset frequencies and verify the correct output frequency.

OFFSET FREQUENCY (MHz)	DUPLEX FREQUENCY (MHz)
+1.0000	151.0000
-2.0000	148.0000
+5.5000	155.5000
-10.0000	140.0000
+15.5500	165.5500
-20.0000	130.0000
+35.0000	185.0000
-49.9900	100.0100

9. Disconnect Frequency Counter and connect Spectrum Analyzer to DUPLEX Connector (14). Verify the output level is -60 dBm (±10 dB).

10. Connect Spectrum Analyzer to T/R Connector (11) and verify the output level is -80 dBm (±5 dB).

11. Disconnect all test equipment.

12. Place MODE Selector Control (39) to "GEN" Position. Using RF Level Attenuator Vernier Control (10), set FM/AM-1200 for an output level of -40 dBm.

13. Connect Frequency Counter to T/R Connector (11).

STEP	PROCEDURE

14. Using Keyboard (18), select the following frequencies and verify the output frequency at the T/R Connector (11), as given below:

SELECTED FREQUENCY	OUTPUT FREQUENCY (Frequency Counter Reading)
RF 0.6666 MHz	0.6666 MHz
RF 1.9999 MHz	1.9999 MHz

15. Disconnect Frequency Counter.

SECTION 4 - CALIBRATION

4-1 GENERAL

This section contains calibration procedures for the following FM/AM-1200 front panel indicators and internal modules:

CALIBRATION PROCEDURE	CALIBRATION PROCEDURE TITLE	PAGE NO
4-2-1	Mechanical Zero of Meters	4-7
4-2-2	Power Supply Calibration	4-9
4-2-3	Frequency Standard Calibration	4-11
4-2-4	Function Generator Calibration	4-13
4-2-5	High Loop Calibration	4-15
4-2-6	Digital Module Calibration	4-19
4-2-7	Modulation Meter Calibration	4-21
4-2-8	Generate Signal Calibration	4-25
4-2-9	DVM I/O Calibration	4-29
4-2-10	Oscilloscope/Analyzer Calibration	4-31

These procedures should be performed as a result of one or more of the following conditions:

1. If, during the course of normal operation, the FM/AM-1200 fails to meet the performance specifications as provided in "SECTION 3 - PERFORMANCE EVALUATION".

2. If a module is found to be defective and requires significant repair or replacement.

3. If the recommended annual calibration is due.

4-1-1 SAFETY PRECAUTIONS

As with any piece of electronic equipment, extreme caution should be taken when troubleshooting "live" circuits. When performing the calibration procedures in this section, be sure to observe the following precautions:

WARNING

AS LONG AS THE BATTERY IS INSTALLED OR EXTERNAL AC OR DC POWER IS APPLIED, A 12 VDC POTENTIAL EXISTS AT VARIOUS POINTS ON REAR PANEL, REGARDLESS OF THE FRONT PANEL POWER SWITCH POSITION.

WARNING

WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL, KEEP ONE HAND IN POCKET OR BEHIND YOUR BACK TO AVOID SERIOUS SHOCK HAZARD.

REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE TROUBLESHOOTING AND/OR REPAIRING LIVE CIRCUITS.

FOR ADDED INSULATION, PLACE RUBBER BENCH MAT UNDER ALL POWERED BENCH EQUIPMENT, AS WELL AS A RUBBER FLOOR MAT BENEATH TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

4-1-2 DISASSEMBLY REQUIREMENTS

To perform any of the calibration procedures contained in this section (with the exception of 4-2-1, Mechanical Zero of Meters), the exterior case must be removed from the FM/AM-1200. The only modules which must be removed and disassembled specifically for calibration are the three Spectrum Analyzer Modules. Refer to Section 6 for mechanical illustrations of the FM/AM-1200 and its various subassemblies.

4-1-3 TEST EQUIPMENT REQUIREMENTS

A list of test equipment required to perform each calibration procedure is provided with the procedure. The minimum equipment specifications which can meet the requirements for the procedure are listed in Appendix B.

4-1-4 CONTROLS AND CALIBRATION POINTS

The various front and rear panel controls, connectors and indicators specified in the calibration procedures are followed by an item number. Figure 1-2 shows the location of each of these items. Calibration points for the Spectrum Analyzer Module are shown on the individual PC Board drawings in Section 7. All other calibration points are identified in Figure 4-5.

4-1-5 UPON COMPLETION OF CALIBRATION PROCEDURES

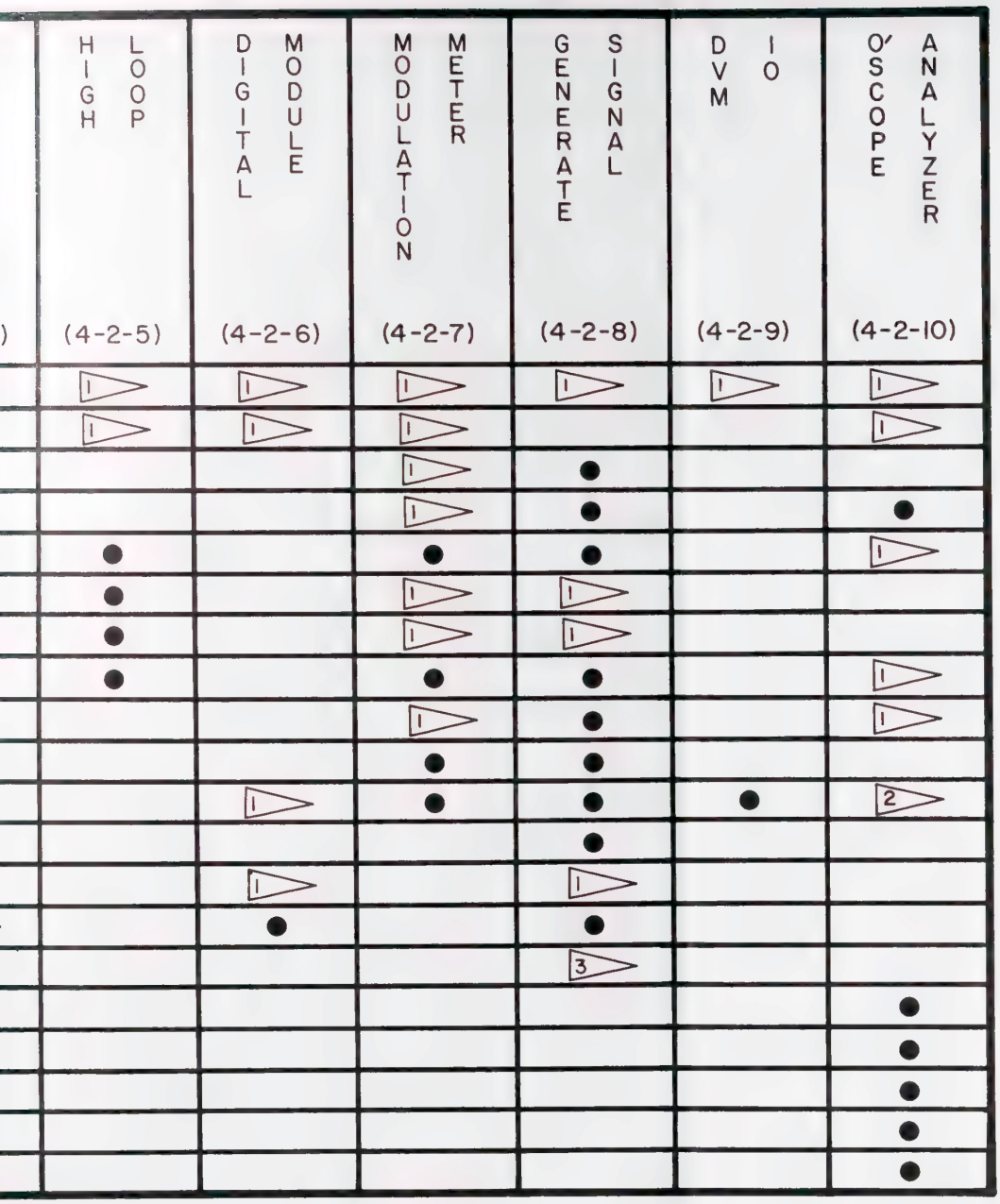
The procedures contained in this section are complete for the system specifically addressed, and upon completion of a given procedure, the entire calibration procedure may be terminated. Control settings, operating commands, and test equipment connections do not carry over from one procedure to another, and are not assumed at the start of any procedure. Always disconnect all test equipment and reconnect any cables, harnesses, etc., (which may have been disconnected or removed while conducting a procedure) upon its completion.

4-2 CALIBRATION PROCEDURES

Before making any calibration adjustments, always observe the signal measurement. If the measurement is within the tolerances given, do not proceed with that specific adjustment. (The only time an adjustment is required for a measurement that is within tolerance is when a subsequent interactive adjustment is insufficient and the procedure explicitly requires repeating previous steps.) Normally, when an adjustment is required, the technician should attempt to obtain a precise measurement, and not be satisfied with an adjustment that is just within tolerance.

IF THIS MODULE IS REPAIRED OR REPLACED / THEN THE FOLLOWING CALIBRATION PROCEDURES MUST BE PERFORMED	MECH ZERO OF METERS (4-2-1)	POWER SUPPLY (4-2-2)	FREQUENCY STANDARD (4-2-3)	(
POWER SUPPLY	1	●	1	
FREQUENCY STANDARD PC BD.			●	
OUTPUT AMPLIFIER MODULE				
IF MODULE				
DUAL VCO MODULE				
1120 MHz LOW PASS FILTER				
HIGH/LOW PASS FILTER				
HIGH LOOP MODULE				
LOW LOOP MODULE				
10.7 MHz GEN/REC MODULE				
RECEIVE AUDIO PC BD.				
GENERATE AUDIO PC BD.				
TONE GENERATOR PC BD.				
DIGITAL MODULE				
DUPLEX GENERATOR				
O'SCOPE CONTROL PC BD.				
CRT POWER SUPPLY PC BD.				
ANALYZER RF MODULE				
ANALYZER IF MODULE				
ANALYZER LOG AMP MODULE				

●	CALIBRATION REQ
1	CALIBRATION REQ PERFORMANCE EVA
2	COMPLETE STEPS PROCEDURE 4-2-1
3	COMPLETE STEPS PROCEDURE 4-2-8



LEGEND
D
ED ONLY IF MODULE FAILS TION.
THRU 31 IN CALIBRATION
THRU 21 IN CALIBRATION

Figure 4-1 Module Replacement & Alignment Requirements

4-2-1 MECHANICAL ZERO OF METERS

PREREQUISITES: None

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Small Slotted Screwdriver

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
3	Modulation Meter Zero Adjustment	As is
22	PWR/OFF/BATT Switch	"OFF" (Battery Power Off)
38	Frequency Error Meter Zero Adjustment	As is

STEP	PROCEDURE
1.	Rotate each adjustment (3, 38) cw or ccw as required to position the appropriate meter needle directly over the "0" on the meter scale.

4-2-2 POWER SUPPLY CALIBRATION

PREREQUISITES: None

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)
1 Non-Conductive Tuning Tool
1 Digital Multimeter
1 Battery Load Simulator (Ref. Appendix D)

INITIAL CONTROL SETTINGS: See Figure 1-2

CONTROL	INITIAL SETTINGS
22 PWR/OFF/BATT Switch	"OFF" (Battery Off) Position

CALIBRATION POINTS: See Figure 4-5

STEP PROCEDURE

1. With external power disconnected, remove test set from its case.

2. Connect test set to appropriate AC line supply, then place test set on its Rear Panel (Front Panel facing up). Place PWR/OFF/BATT Switch (22) in "PWR" position.

3. On the Battery Charger PC Board, verify the voltage between E3 and ground (E1) is a minimum of +14 VDC.

4. Verify voltage at E7 is +12 VDC (±.1V). Adjust R3901, as needed, to bring the voltage into tolerance.

5. Verify the following voltages are within tolerance:

TEST POINT	VOLTAGE
E4	+5.1 VDC (±.2V)
E5	-12 VDC (±.5V)
E6	+40 to +50 VDC

NOTE

Adjust R3901, as needed, to bring any of the above listed voltages into tolerance.

6. Disconnect the battery and connect a Battery Load Simulator across the pins of J1702. Set Battery Load Simulator for 300 mAmps.

7. Verify the voltage across the Battery Load Simulator is +14.4 VDC (±.1V). Adjust R1604, as needed, to bring the voltage into tolerance.

8. Disconnect all test equipment.

4-2-3 FREQUENCY STANDARD CALIBRATION

PREREQUISITES: Power Supply Calibration Procedure 4-2-2

SPECIAL ACCESSORY EQUIPMENT REQ'D:
(See Appendix B for Test Equipment Requirements)
1 Non-Conductive Tuning Tool
1 Digital Multimeter
1 Frequency Counter

INITIAL CONTROL SETTINGS: See Figure 1-2

CONTROL	INITIAL SETTINGS
22 PWR/OFF/BATT Switch	"PWR" Position

CALIBRATION POINTS: See Figure 4-5

STEP PROCEDURE

1. After a 15-minute warmup period (30-minutes for Opt-02), connect frequency counter to the 10 MHz External Reference Connector (45) and a digital voltmeter to pin 2 (wiper) of REF CAL potentiometer (13).

2. Verify frequency is 10 MHz (±.1 Hz) and voltage is +5.5 VDC (±2.0V) (+2.5 VDC (±1.0V) if oven oscillator is installed). Adjust R3501, if necessary, to obtain the correct frequency. If the correct frequency cannot be obtained within the voltage tolerance, proceed with Steps 3 through 5.

3. Reset voltage at pin 2 of R3501 to +5.5 VDC for TCXO or +2.5 VDC for oven oscillator.

4. Remove adjustment access screw from the TCXO or oven oscillator. Adjust the oscillator to obtain a frequency of 10 MHz ±.5 Hz (±.1 Hz if possible). Replace adjustment access screw.

5. If further fine adjustment is required, adjust R3501 as required to obtain a frequency of 10 MHz (±.1 Hz).

6. Disconnect all test equipment.

4-2-4 FUNCTION GENERATOR CALIBRATION

PREREQUISITES: Power Supply Calibration Procedure 4-2-2
Frequency Standard Calibration Procedure 4-2-3

SPECIAL ACCESSORY EQUIPMENT REQ'D: (See Appendix B for Test Equipment Requirements)
1 Non-Conductive Tuning Tool
1 Frequency Counter
1 Distortion Analyzer
1 Digital Multimeter
1 Tone Generator Extender Board
1 150Ω 1/2 W Resistor

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
5	VAR Tone Selector Switch	"OFF" Position
6	VAR Tone Level Control	Fully ccw Position
7	1 kHz Tone Selector Switch	"OFF" Position
8	1 kHz Tone Level Control	Fully ccw Position
22	PWR/OFF/BATT Switch	"PWR" Position
39	MODE Selector	"REC" Position
40	VOLUME Control	Fully ccw Position
41	SQUELCH Control	Fully ccw Position

CALIBRATION POINTS: See Figure 4-5

STEP PROCEDURE

1. Connect 150Ω 1/2 W resistor across TONE OUT Connector (17) on Front Panel. Connect True RMS Voltmeter and Distortion Meter across the resistor.

2. Set 1 kHz Tone Selector Switch (7) in "INTL" position and rotate 1 kHz Tone Level Control (8) to obtain 2.5 VRMS. Verify distortion is less than 0.5%.

3. Set 1 kHz Tone Selector Switch (7) in "OFF" position and VAR Tone Selector Switch (5) in "INTL" position.

4. Using Keyboard (18), select TONE, 5000.0 Hz SINE.

5. Adjust VAR Tone Level Control (6) to obtain 2.5 VRMS.

6. Connect Frequency Counter to TONE OUT Connector (17) and verify frequency is 5000.0 Hz (± 0.5 Hz). If frequency is within tolerance, omit Step 7.

STEP	PROCEDURE
7.	If frequency at Step 6 is not within tolerance, set the PWR/OFF/BATT Switch (22) to the "OFF" position and proceed as follows:
	a. Remove the Function Generator PC Board and install Extender Cable in its place, then install the Function Generator PC Board on the Extender Cable.
	b. Set PWR/OFF/BATT Switch (22) to "PWR" position.
	c. Verify test set is in the TONE mode, producing a 5000.0 Hz sinewave at 2.5 VRMS across the 150Ω resistor.
	d. With the Frequency Counter connected to the TONE OUT Connector (17), adjust C3110 on the Function Generator PC Board to obtain a frequency of 5000.0 Hz (±0.5 Hz).
8.	With the Distortion Analyzer connected across the 150Ω resistor, verify distortion is less than 0.7%.
9.	Using Keyboard (18), select TONE, 1000.0 Hz SINE.
10.	Verify the signal level is 2.5 VRMS. Adjust VAR Tone Level Control (6), if necessary, to obtain desired reading.
11.	Verify distortion is less than 0.7%.
12.	Disconnect Distortion Analyzer.
13.	Set the FM/AM-1200 controls as follows:

	CONTROLS	INITIAL SETTINGS
5	VAR Tone Selector Switch	"INTL" Position
6	VAR Tone Level Control	"1 kHz" Position
24	VERTICAL Attenutor Selector Control	"2 kHz/Div" Position
26	HORIZONTAL Sweep Selector Control	".1 mS/Div Position
39	MODE Selector Control	"GEN" Position

14.	Using Keyboard (18), verify Sine, Ramp, Square and Triangle waveforms are displayed on both VFD (37) and CRT (31).

4-2-5 HIGH LOOP CALIBRATION

PREREQUISITES:
Meter Zero Calibration Procedure 4-2-1
Power Supply Calibration Procedure 4-2-2
Frequency Standard Calibration Procedure 4-2-3

SPECIAL ACCESSORY EQUIPMENT REQ'D:
(See Appendix B for Test Equipment Requirements)
1 Non-Conducting Tuning Tool
1 40 VDC Power Supply
1 Frequency Counter
1 Digital Multimeter
1 Spectrum Analyzer
1 2 to 3 Foot Coax Cable with BNC/SMB Connectors
1 Coax with BNC/BNC Connectors
1 BNC Tee Connector
1 Tune Control Pot (See Appendix D)
1 Coax Jumper SMB/SMB Female Connectors
2 2 to 3 Foot Coax Cables with SMB/SMB Connectors

INITIAL CONTROL SETTINGS:
See Figure 1-2

CONTROL	INITIAL SETTINGS
22 PWR/OFF/BATT Switch	"PWR" Position

CALIBRATION POINTS:
See Figure 4-5

STEP PROCEDURE

1. Disconnect P/J1903 and P/J1902 on the Dual VCO.
2. Connect Frequency Counter to J1902.
3. Verify frequency is 1210 MHz (±1 MHz). Adjust C2003, if necessary, for correct frequency.

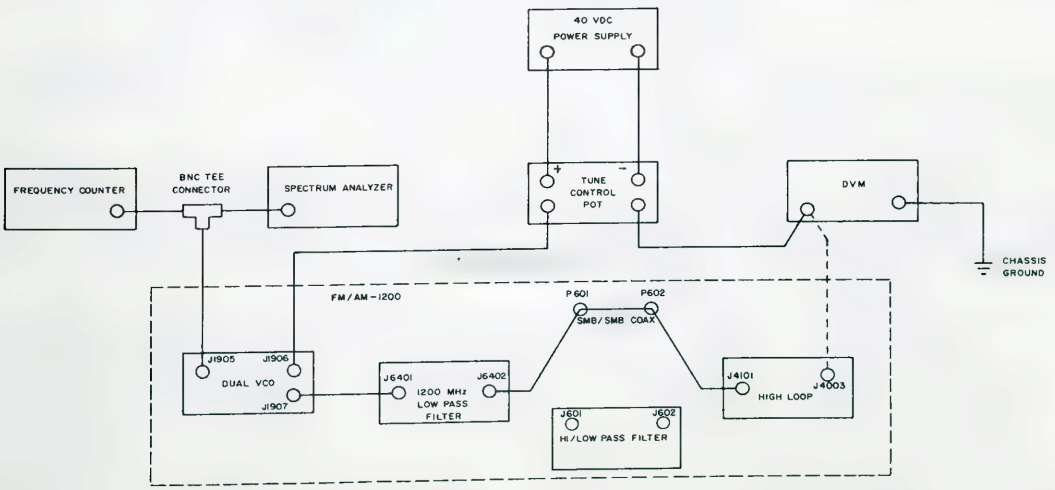


Figure 4-2 High Loop Calibration Set-up

STEP	PROCEDURE
4.	Connect Test Equipment as shown in Figure 4-2.
5.	Select RF 299.0000 on the FM/AM-1200 Keyboard (18).
6.	Adjust the Tune Control Pot to obtain the following VCO frequencies and record the corresponding DC voltages: a. 2330 MHz b. 1275 MHz
7.	Disconnect the DVM from the VCO Tune Control Pot and connect it to J4003 on the High Loop.
8.	With the VCO tuned below 1598 MHz, verify the DC voltage of J4003 corresponds with the voltage recorded in step 6.a. (2330 MHz). Adjust R4061, if necessary, to obtain the correct voltage.
9.	With the VCO tuned above 1800 MHz, verify the DC voltage at J4003 corresponds with the voltage recorded in step 6.b. (1275 MHz). Adjust R4060, if necessary, to obtain the correct voltage.
10.	Verify the VCO output level at J1905 is +5 to +12 dBm.
11.	Disconnect all test equipment and reconnect P/J1906 and P/J4003. Verify the PHASE LOCK Indicator on the High Loop is not illuminated.
12.	Connect DVM to FL601 on the Hi/Low pass filter.
13.	Using the Keyboard (18), select RF 450.0000 MHz. Verify DVM displays approximately +10 VDC.
14.	Using the Keyboard (18), slew the frequency upward in 10 MHz increments until the DVM reading switches from approximately +10 VDC to approximately -10 VDC. Verify switching occurs between 450 and 490 MHz as indicated on the Front Panel Display (37). Record the switching frequency. If switching occurs within this range, omit steps 15 through 17. If not, proceed as follows.
15.	Select RF 490.0000 MHz on the Keyboard (18). Verify DVM indicates approximately -10 VDC. If necessary, rotate R4065 ccw until this reading is obtained.
16.	Repeat steps 13 and 14 to verify switching from -10 VDC to +10 VDC now occurs between 450 and 490 MHz. If necessary, repeat steps 15 through 17, slightly altering R4065 each time.

STEP PROCEDURE

17. Using SMB Tee Connector, connect Spectrum Analyzer to J4101. Reconnect P/J601 and P/J602. Verify Hi/Low Pass Filter output is -35 dBm or greater at the frequencies listed below:

SELECTED FREQUENCY	ANALYZER CENTER FREQUENCY
RF 200.000 MHz	290 MHz
RF 800.000 MHz	890 MHz

Disconnect Spectrum Analyzer and reconnect P/J4101.

18. Connect Spectrum Analyzer to J1902 on the Dual VCO. Verify the output is 1210 MHz at +5 to +12 dBm. (Ref. Figure 4-3)

19. Using Keyboard (18), select RF 998.0000 MHz.

20. With Spectrum Analyzer set at 500 KHz/division at 1210 MHz, adjust R4032 on the High Loop for the lowest level of sidebands. Disconnect Spectrum Analyzer and reconnect P/J1902.

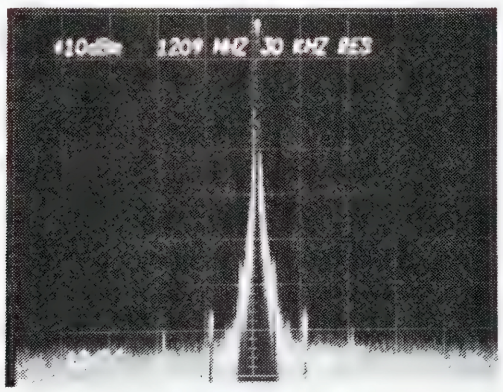


Figure 4-3 DUAL VCO 1210 MHz Output

21. Connect Spectrum Analyzer to J4103 on the High Loop. Verify output level is -20 dBm (±5 dB) at 1088 MHz. (Ref. Figure 4-4)

22. Using Keyboard (18) select RF 050.0000 MHz. With Spectrum Analyzer set at 10 kHz/division and 140 MHz, center frequency, verify the High Loop output level is -20 dBm (±5 dB).

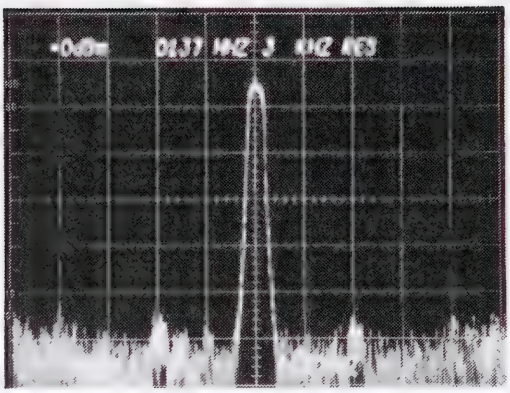


Figure 4-4 DUAL VCO 90 MHz to 1080 MHz Output

23. Adjust R4045 as necessary to obtain flat sidebands.

24. Disconnect Spectrum Analyzer and reconnect all cables.

25. Using Keyboard (18), select the following frequencies and verify the noise floor level rises no more than 6 dB on the sidebands. Perform Steps 19 through 23 only if this level is not obtained.

SELECTED FREQUENCY	ANALYZER CENTER FREQUENCY
RF 250.0000 MHz	340 MHz
RF 450.0000 MHz	540 MHz
RF 850.0000 MHz	940 MHz

26. Disconnect Spectrum Analyzer and connect Frequency Counter to J4103.

27. Verify digit operation on frequency counter with FM/AM-1200 frequency selection as shown below:

FM/AM-1200 Frequency	DUAL VCO Output Frequency (J4103)
666.0000 MHz	756 MHz
998.0000 MHz	1088 MHz

4-2-6 DIGITAL MODULE CALIBRATION

PREREQUISITES: Meter Zero Calibration Procedure 4-2-1
Power Supply Calibration Procedure 4-2-2
Frequency Standard Calibration Procedure 4-2-3

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Non-Conductive Tuning Tool
1 2 to 3 Foot Coax Cable with BNC/BNC Connector

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
5	VAR Tone Switch	"OFF" Position
7	1 kHz Tone Switch	"OFF" Position
22	PWR/OFF/BATT	"PWR" Position
35	FREQ ERROR Selector	"10 kHz" Position
39	MODE Selector	"REC" Position
40	VOLUME Control	Fully ccw Position
41	SQUELCH Control	Fully ccw Position

CALIBRATION POINTS: See Figure 4-5

STEP PROCEDURE

1. Select RF 10.0000 MHz on keyboard (180.
2. Connect the coax cable to the ANT Connector (34) and the 10 MHz External Reference Connector (45).
3. Verify Frequency Error Meter (36) reads "0". Adjust R4407, if necessary, to position the needle directly over the "0" point.
4. Select RF 10.0100 MHz on the Keyboard (18).
5. Verify Frequency Error Meter (36) reads full scale negative deflection (-1 on the upper scale). Adjust R4510, if necessary, to obtain the current reading.
6. Select RF 10.0030 MHz on the Keyboard (18).
7. Rotate FREQ ERROR Meter Selector (35) to the 3K position.
8. Verify Frequency Error Meter (36) reads full scale negative deflection (-3 on the upper scale). Adjust R4509, if necessary, to obtain the correct reading.
9. Disconnect all test equipment.

4-2-7 MODULATION METER CALIBRATION

PREREQUISITES:
Meter Zero Calibration Procedure 4-2-1
Power Supply Calibration Procedure 4-2-2
Frequency Standard Calibration Procedure 4-2-3

SPECIAL ACCESSORY EQUIPMENT REQ'D:
(See Appendix B for Test Equipment Requirements)
1 Non-Conductive Tuning Tool
1 RF Signal Generator with Attenuator
1 Oscilloscope
1 Distortion Analyzer
1 Digital Multimeter
1 Modulation Meter
1 5 Watt Transmitter
1 30 Watt Transmitter

INITIAL CONTROL SETTINGS:
See Figure 1-2

	CONTROL	INITIAL SETTINGS
2	MODULATION Selector	"FM NAR" Position
4	Modulation METER Selector	"AVG 15" Position
5	VAR Tone Selector Switch	"OFF" Position
7	1 kHz Tone Selector Switch	"OFF" Position
9	GEN LEVEL Vernier	Fully ccw Position
10	GEN LEVEL Attenuator	"-20 dBm" Position
18	Keyboard	"RF 120.2 MHz" Position
22	PWR/OFF/BATT Switch	"PWR" Position
39	MODE Selector	"GEN" Position

CALIBRATION POINTS:
See Figure 4-5

STEP PROCEDURE

1. Verify modulation reads zero on MODULATION METER (1), adjust R3454, as necessary, to obtain zero reading.

2. Connect 5 Watt Transmitter to T/R Connector (11). Key Transmitter and verify MODULATION METER (1) reads 5 W Avg (see Specifications in Appendix A). Adjust R3365, as necessary, to obtain correct reading. Disconnect Transmitter.

3. Place Modulation METER Control (4) to "AVG 150" Position.

4. Connect 30 Watt Transmitter to T/R Connector (11). Key Transmitter and verify Modulation METER (1) reads 30 W Avg (see Specifications in Appendix A). Adjust R3362, as necessary, to obtain correct reading. Disconnect Transmitter.

5. Place Modulation METER Control to "BATT" Position.

STEP	PROCEDURE
6.	Connect Multimeter to J1601, Pin 5 on Battery Charger PC Board. Verify reading on MODULATION METER (1) is the same as the Multimeter. Adjust R3303, as necessary to obtain correct reading. BAT. CAL
7.	Place MODULATION Select Control (3) to "FM NAR" Position and Modulation METER Control (4) to "2 kHz" Position.
8.	Verify MODULATION METER (1) on FM/AM-1200 indicates zero. Adjust R3368, if necessary, to position the needle directly over the zero division mark.
9.	Set MODE Selector Control (39) to "REC" Position.
10.	Adjust RF Signal Generator to produce an unmodulated signal of 120.2 MHz at -50 dB, then connect it to the FM/AM-1200 ANT Connector (34).
11.	Calibrate the modulation function of the MODULATION METER (1) as follows. Refer to Table 4-1, Test Sequences 1 through 9.
	a. For each test sequence, set RF Signal Generator as shown in Table 4-1.
	b. Set FM/AM-1200 as shown in Table 4-1 and verify the reading is within tolerance. Adjust the specified trimpot as required to obtain the correct reading.
12.	Verify FM/AM-1200 demodulation distortion as follows. Refer to Table 4-1, Test Sequences 10 through 12.
	a. Using Coax "Tee", connect Digital Multimeter to DEMOD Connector (16) of FM/AM-1200.
	b. For each test sequence, set RF Signal Generator as shown in Table 4-1.
	c. Set FM/AM-1200 as shown in Table 4-1.
	d. Connect Distortion Meter to DEMOD Connector (16) of FM/AM-1200, using the Coax Tee, and measure distortion. The observed distortion, should be less than the maximum given in Table 4-1 for the appropriate test sequence.
13.	Disconnect the RF Signal Generator.

STEP	PROCEDURE

14. Set the FM/AM-1200 controls as follows:

	CONTROL	INITIAL SETTINGS
4	METER Selector	"DIST" Position
5	VAR Tone Selector Switch	"OFF" Position
7	1 kHz Tone Selector Switch	"INTL" Position
8	1 kHz Level Control	Fully cw Position
39	MODE Selector	"REC" Position

15. Connect coax cable from Tee on TONE OUT Connector (17) to EXT MOD/SINAD Connector (15).

16. Verify MODULATION Meter (1) indicates minimum distortion (distortion must be less than or equal to 5%). Adjust R3318 and R3320 as necessary to obtain maximum deflection.

17. Adjust 1 kHz Tone Level Control (8) for 1.999 VRMS on Digital Multimeter.

18. Set 1 kHz Tone Selector Switch (7) in "OFF" position and VAR Tone Selector Switch (5) in "INTL" position. Using Keyboard (18) select a variable tone of 1000 Hz Sinewave.

19. Adjust the VAR Tone Level Control (6) for .199 VRMS on Digital Multimeter.

20. Place 1 kHz Tone Selector Switch (7) to "INTL" Position and Modulation METER Control (4) to "DIST" Position. Verify MODULATION METER (1) displays 10% distortion. Adjust R3350, as necessary to obtain correct reading.

21. Place 1 kHz Tone Selector Switch (7) to "OFF" Position and adjust VAR Tone Level Control (6) for .500 VRMS on Digital Multimeter.

22. Place 1 kHz Tone Selector Switch (7) to "INTL" Position and Modulation Meter Control (4) to "SINAD" Position. Verify MODULATION METER (1) reads 12 dB SINAD.

23. Disconnect all test equipment.

RF SIGNAL GENERATOR				FM/AM-1200						
TEST SEQ NO.	MOD MODE	TONE FREQ	MOD DEV/%	MODULATION SELECTOR SETTING	METER SELECTIVE SETTING kHz/%x10	METER READING	TOL. ±	ADJUST	DEMOD OUTPUT LEVEL VP-P	FM/AM-1200 DISTORTION LESS SIGNAL GENERATOR DISTORTION	REMARKS
1	FM	1K	0	FM NAR	2	0	0	R3369			
2	FM	1K	0	FM WIDE	2	0	0	R3370			
3	FM	1K	5K	FM NAR	6	5	±.43 kHz	R3303			
4	Repeat Test Sequences 1, 2 and 3 as required to obtain proper readings										Sequences 1, 2 and 3 are interactive
5	FM	1K	1.5K	FM NAR	2	1.5	±.135 kHz	None			Verify Only
6	FM	1K	50K	FM MID	60	5	±4.3 kHz	None			Verify Only
7	AM	1K	0	AM NORM	2	0	0	R3371			
8	AM	1K	80%	AM NORM	20	.8	±10% AM	R3379			
9	Repeat Test Sequences 7 and 8 as required to obtain proper readings										Sequences 7 and 8 are interactive
10	FM	1K	5K	FM NAR	6				.85	<3%	Verify Only
11	FM	1K	20K	FM MID	60				8.5	<2%	Verify Only
12	AM	1K	80%	AM NORM	20				1.12	<4%	Verify Only

Table 4-1 Modulation Meter Calibration Requirements

4-2-8 GENERATE SIGNAL CALIBRATION

PREREQUISITES:
Meter Zero Calibration Procedure 4-2-1
Power Supply Calibration Procedure 4-2-2
Frequency Standard Calibration Procedure 4-2-3
Function Generator Calibration Procedure 4-2-4
High Loop Calibration Procedure 4-2-5
Digital Calibration Procedure 4-2-6

SPECIAL ACCESSORY EQUIPMENT REQ'D:
(See Appendix B for Test Equipment Requirements)
1 Non-Conductive Tuning Tool
1 Microphone
1 Function Generator
1 Power Meter
1 Oscilloscope
1 Spectrum Analyzer
1 Modulation Meter

INITIAL CONTROL SETTINGS: See Figure 1-2

	CONTROL	INITIAL SETTINGS
3	MODULATION Select Control	"AM NORM" Position
5	VAR Tone Selector Switch	"OFF" Position
7	1 kHz Tone Selector Switch	"OFF" Position
9	GEN LEVEL Attenuator	"-20 dBm" Position
10	GEN LEVEL Vernier	Fully ccw Position
22	PWR/OFF/BATT Switch	"PWR" Position
32	GEN/LOCK Control	"LOCK" Position
39	MODE Selector	"GEN" Position

CALIBRATION POINTS: See Figure 4-5

STEP PROCEDURE

1. Using keyboard (18), enter "RF 120.0000" MHz.

2. Connect Spectrum Analyzer to T/R Connector (11).

3. Vary GEN LEVEL Vernier Control (10) smoothly throughout its full range and verify the output level observed on the Spectrum Analyzer tracks.

4. Connect Modulation Meter to T/R Connector (11). Set RF Level Attenuator Control (9) fully "CCW" and 1 kHz Tone Level Control (8) for 50% AM modulation on MODULATION METER (1). Set RF Level Attenuator Vernier Control (10) fully clockwise and verify AM modulation on MODULATION METER (1) over range reads 50% modulation (±5%). Adjust R5114, as necessary, through the access hole in the Output Amplifier Module, to obtain the desired reading.

5. Disconnect Modulation Meter and connect Power Meter to T/R Connector (11).

STEP PROCEDURE

6. Using only the GEN LEVEL Vernier Control (10), make the following output level settings and verify the output levels on the Power Meter are within ±0.5 dB. If necessary, make the corresponding adjustments, listed below, to obtain the correct level. Repeat these three adjustments, as necessary, until all are within tolerance.

Setting	Adjustment
a. -31 dBm	R3224
b. -42 dBm	R3246
c. -37 dBm	R3227

7. Rotate GEN LEVEL Vernier Control (10) to -31 dBm. Select the following RF frequencies on the Keyboard (18) and verify the corresponding Power Meter readings are -31 dBm (±2.5 dB).

200 MHz	500 MHz	800 MHz	1 MHz
300 MHz	600 MHz	900 MHz	10 MHz
400 MHz	700 MHz	999 MHz	100 MHz

8. Connect Function Generator to EXT MOD/SINAD Connector (15).

9. Adjust Function Generator output for a 1 kHz tone at 1 VRMS. Verify MODULATION Meter (1) shows 50% (±15%).

10. Set MODULATION Select Control (3) to "FM MID" Position and MODULATION Meter Control (4) to "20 kHzx10" Position.

11. Adjust Audio Signal Generator output to 3 VRMS at 1 kHz. Verify MODULATION METER (1) displays 15 kHz (±4.5 kHz). Disconnect Signal Generator from EXT MOD/SINAD Connector (15).

12. Connect Microphone to MIC/ACC Connector (19). Speak into Microphone and verify that MODULATION Meter (1) peaks no greater than 6 kHz deviation.

13. Rotate the GEN/LOCK Control (32) out of the detent. Verify the LOCK Lamp (33) flashes and the FREQ ERROR Meter (36) indicates a minimum error of -10 kHz.

14. Rotate the GEN/LOCK Control (32) fully cw and verify the FREQ ERROR Meter (36) indicates a minimum error of +10 kHz.

15. Rotate the GEN/LOCK Control (32) fully ccw into "LOCK" position. Verify the LOCK Light (33) becomes steady.

STEP	PROCEDURE

16. Set Spectrum Analyzer to 20 MHz/Div and connect to T/R Connector (11). Verify non-harmonic frequencies are a minimum of 40 dBc at the following frequencies:

    600 MHz 700 MHz 470 MHz 120 MHz

17. Rotate MODE Selector (39) to "DUP" position.

18. Using Keyboard (18) select RF 070.0000 MHz, set OFFSET to 00.0 and verify Spectrum Analyzer indicates -80 dBm (±5 dB).

19. Connect Spectrum Analyzer to DUPLEX Connector (14) and verify output level is -60 dBm (±10 dB).

20. Using BNC to BNC Coax Cable, connect DUPLEX Output Connector (14) to ANT Connector (34). Set MODE Selector Control (39) to "DUP GEN" Position and 1 kHz Tone Selector Switch (7) to "INTL" Position. Adjust 1 kHz Tone Level Control (8) for 5 kHz deviation on MODULATION METER (1).

21. Set MODE Selector Control (39) to "DUP" Position and verify 5 kHz deviation is displayed on MODULATION METER (1). Adjust R1224, as necessary, to obtain desired deviation.

NOTE

Repeat this procedure until 5 kHz deviation is obtained on both scales.

22. Disconnect all test equipment.

4-2-9 DVM I/O BOARD CALIBRATION

PREREQUISITES:
Meter Zero Calibration Procedure 4-2-1
Power Supply Calibration Procedure 4-2-2
Frequency Standard Calibration Procedure 4-2-3
Function Generator Calibration Procedure 4-2-4
High Loop Calibration Procedure 4-2-5
Digital Module Calibration Procedure 4-2-6

SPECIAL ACCESSORY EQUIPMENT REQ'D:
(See Appendix B for Test Equipment Requirements)

1 RF Signal Generator
1 Coax Cable, BNC to BNC

INITIAL CONTROL SETTINGS:
See Figure 1-2

	CONTROL	INITIAL SETTINGS
2	MODULATION SELECTOR	"FM NAR" Position
4	METER Range Selector	"2 kHz/%X10" Position
5	VAR Tone Selector Switch	"OFF" Position
7	1 kHz Tone Selector Switch	"OFF" Position
22	PWR/OFF/BATT Switch	"PWR" Position
35	FREQ ERROR Selector	"RF 10K" Position
39	MODE Selector	"GEN" Position
41	SQUELCH Control	Fully ccw Position

CALIBRATION POINTS:
See Figure 4-5

STEP PROCEDURE

1. Using the Keyboard (18) select RF 151.0000 MHz and 2ND FUNCTION METER.

2. Adjust R3021 as required for a reading of "MD 00.00" on VFD (37).

3. Place Modulation METER Control (4) to "6 kHz" Position and 1 kHz Tone Selector Switch to "INTL" Position. Adjust 1 kHz Tone Level Control (8) for 5 kHz deviation on MODULATION METER (1).

4. Verify the VFD (37) reads "MD 5.00" ±.60. Adjust R3007, as required, for the correct display.

5. Set MODE Selector Control (39) to "REC" Position and using Keyboard select "RF 9.9950 MHz" on VFD (37).

6. Connect BNC to BNC Coax Cable between ANT Connector (34) and External Reference Connector (45).

7. Verify VFD (37) reads "FE + 05.00" (±.30). Adjust R3002, as required, to obtain the proper reading.

STEP	PROCEDURE
8.	Place Modulation METER Control (4) to "2 kHz" Position and verify VFD (37) displays between "3.07 and 3.10". Adjust, as required, R3008 for correct reading on VFD (37).
9.	Disconnect all test equipment.

4-2-10 OSCILLOSCOPE/ANALYZER CALIBRATION

PREREQUISITES:
Meter Zero Calibration Procedure 4-2-1
Power Supply Calibration Procedure 4-2-2
Frequency Standard Calibration Procedure 4-2-3
Function Generator Calibration Procedure 4-2-4
High Loop Calibration Procedure 4-2-5
Digital Module Calibration Procedure 4-2-6
Modulation Meter Calibration Procedure 4-2-7

SPECIAL ACCESSORY EQUIPMENT REQ'D:
(See Appendix B for Test Equipment Requirements)
1 Non-Conductive Tuning Tool
1 Digital Multimeter
1 RF Signal Generator
1 DC Power Supply
1 Coax Cable, BNC to BNC

INITIAL CONTROL SETTINGS:
See Figure 1-2

	CONTROL	INITIAL SETTINGS
23	VERTICAL Vernier Control	"CAL" Position
24	VERTICAL Selector Control	"1 V/DIV" Position
25	HORIZONTAL Vernier Control	"CAL" Position
26	HORIZONTAL Selector Control	"TONE" Position
22	PWR/OFF/BATT Switch	"PWR" Position
27	VERT POS Control	Midrange Position
28	INT Control	Midrange Position
29	FOCUS Control	Midrange Position
30	HORIZ POS Control	Midrange Position
39	MODE Selector Control	"GEN" Position

CALIBRATION POINTS:
See Figure 4-5

STEP PROCEDURE

1. Verify trace on CRT is a SHARP ROUND DOT. Adjust, as required, Geometry Control, R317 and Astigmatism Control, R316 on Scope Power PC Board for a sharp round dot.

2. Using INT Control (28) and FOCUS Control (29), verify intensity and focus of trace can be properly adjusted. Alternately adjust R317 and R316, if necessary, for proper control of trace.

3. Set VERTICAL Vernier Control (23) to fully CCW Position.

4. Rotate the HORIZONTAL Selector Control (26) to ".1 mS/DIV". Verify the trace is parallel to the horizontal lines on the CRT (31). Adjust R322, as required, to correct any nonparallel condition.

5. Verify trace is positioned over major horizontal axis. Adjust R294, as required, to properly position trace.

STEP	PROCEDURE
6.	Rotate the VERTICAL Vernier Control (23) fully cw and verify the trace does not move. Adjust R215, as necessary, for proper trace operation.
7.	Select RF 151.0000 MHz on the Keyboard (18). Rotate the MODE Selector Control (39) to "GEN" and the HORIZONTAL Selector Control (26) to "1 MHz/DIV".
8.	Using HORIZ POS Control (30), center signal over major vertical axis.
9.	Verify baseline is visible on CRT (31). Adjust R218, as required, until baseline is visible on CRT (31).
10.	Verify trace extends 1 minor division past the left edge of the CRT (31). Adjust R271, as required, for correct trace position.
11.	Verify the trace extends 1 minor division past the right edge of the CRT (31). Adjust R293, as required, for correct trace position.
12.	Repeat Steps 10 and 11 as required for proper trace positioning on CRT (31).
13.	Rotate MODE Selector Control (39) to "REC" position.
14.	Adjust RF Signal Generator for 151.0000 MHz at -50 dBm, with no modulation. Connect Generator to ANTENNA Connector (34) and verify the signal displayed on the CRT (31) is centered on the vertical center line.
15.	Adjust Signal Generator to 147.0000 MHz and verify signal is 4 divisions to the left of center on the CRT (31). Adjust Generator to 155.0000 MHz and verify signal is 4 divisions to the right of center. Adjust R260, as required, for proper dispersion.
16.	Place MODE Selector Control (39) to "GEN" Position and HORIZONTAL Sweep Selector Control (26) to 1 kHz/DIV Position. Adjust R298, as required, to center signal over major vertical axis.
17.	Disconnect the Signal Generator and set the FM/AM-1200 controls as follows:

	CONTROL	INITIAL SETTINGS
23	VERTICAL Vernier Control	"CAL" Position
24	VERTICAL Selector Control	"1V/DIV" Position
25	HORIZONTAL Vernier Control	"CAL" Position
26	HORIZONTAL Selector Control	".01 mS/DIV" Position
39	MODE Selector Control	"REC" Position
21	AC/GND/DC Switch	"DC" Position

STEP PROCEDURE

18. Verify trace is centered over major horizontal axis.

19. Connect Power Supply to SCOPE Connector (20) and apply +4 VDC. Verify trace moves up 4 divisions. Adjust R221, as required, for correct deflection.

20. Rotate VERTICAL Vernier Control (23) fully ccw and verify the trace shows approximately 0.4 V.

21. Set Scope HORIZONTAL Sweep Vernier Control (25) to "CAL" Position.

22. Set AC/GND/DC Switch (21) to "AC" position and verify the trace returns to the center line.

23. Set AC/GND/DC Switch (21) to "GND" position and verify the trace does not move.

24. Disconnect the Power Supply and couple the TONE OUT Connector (17) to the SCOPE Connector (20) with a coax cable.

25. Set the FM/AM-1200 controls as follows:

	CONTROL	INITIAL SETTINGS
5	VAR Tone Selector Switch	"INTL" Position
6	VAR Tone Level Control	Midrange Position
21	AC/GND/DC Switch	"DC" Position
25	HORIZONTAL Vernier Control	".01 mS/DIV" Position

26. Using Keyboard, select "TONE 1000.0 TRIANGLE". Adjust HORIZ POS Control to position first positive peak of signal on leftmost major vertical graticule. Verify each positive peak of the triangle waveform is positioned over each major vertical graticule.

27. Rotate the HORIZONTAL Selector Control (26) to each of the following positions and select the corresponding triangle waveform frequencies with the Keyboard (18). At each selection, verify the CRT (31) shows one cycle per division.

HORIZONTAL SELECTOR	TONE FREQUENCY
a. 10 mS	100 Hz (±10%)
b. 1 mS	1,000 Hz (±10%)
c. .1 mS	10,000 Hz (±10%)

STEP	PROCEDURE

28. With the FM/AM-1200 set from Step 27.c., rotate the HORIZONTAL Vernier Control (23) fully ccw and verify a miminum of 10 cycles per division on the CRT (31). Return the HORIZONTAL Vernier Control (25) to the "CAL" (fully cw) position.

29. Set the FM/AM-1200 Controls as follows:

	CONTROL	INITIAL SETTINGS
2	MODULATION Select Control	"NAR" Position
4	MODULATION Meter Control	"6 kHz/%x10" Position
5	VAR Tone Selector switch	"OFF" Position
7	1 kHz Tone Selector Switch	"INTL" Position
18	Keyboard	"RF 121.0000 MHz" Position
23	VERTICAL Vernier Control	"CAL" Position
24	VERTICAL Selector Control	"2 kHz/%x10" Position
25	HORIZONTAL Vernier Control	"CAL" Position
26	HORIZONTAL Selector Control	"1 mS/DIV" Position
39	MODE Selector Control	"GEN" Position

30. Adjust the 1 kHz Tone Level Control (8) for 4 kHz deviation on the MODULATION Meter (1).

31. Verify the signal displayed on the CRT (31) is 4 divisions peak to peak. Adjust R201, as required, for correct display.
R21

32. Place PWR/OFF/BATT Switch (22) to "OFF" Position, remove coax cable from TONE OUT Connector (17) to SCOPE Connector (20) and connect Signal Generator to ANT Connector (34).

33. Remove Analyzer Log Amp Assembly and apply power to test set.

34. Using VERT POS Control (27) center trace over major horizontal axis.

35. Place 1 kHz Tone Selector Switch (7) to "OFF" Position, VERTICAL Attenuator Selector Control (24) to "1V/Div" Position and Horizontal Sweep Selector Control (26) to "1 MHz/Div" Position.

36. Using HORIZ POS Control (30) center signal over major vertical axis.

37. Place MODE Selector Control (39) to "REC" Position and set Signal Generator to 121.000 MHz @ -40 dBm.

38. Verify CRT (31) displays a signal level of -40 dBm. Adjust R830 and R831 on Analyzer Log Amp PC Board alternately for desired signal level.

39. Adjust R832 to set bottom of the baseline noise floor level at -110 dBm on CRT (31) scale.

STEP	PROCEDURE
40.	Repeat steps 38 and 39 until the peak signal level is set at -40 dBm and noise floor level is set at -110 dBm on CRT (31).

NOTE

If signal level and baseline noise floor cannot be obtained in Step 29, adjust R218 on Scope Control PC Board to obtain desired levels.

41. Set Signal Generator to -70 dBm. Adjust R818 on Analyzer Log Amp PC Board for a signal level of -70 dBm on CRT (31).

42. Set Signal Generator to -90 dBm. Adjust R824 on Analyzer Log Amp PC Board for a signal level of -90 dBm CRT (31).

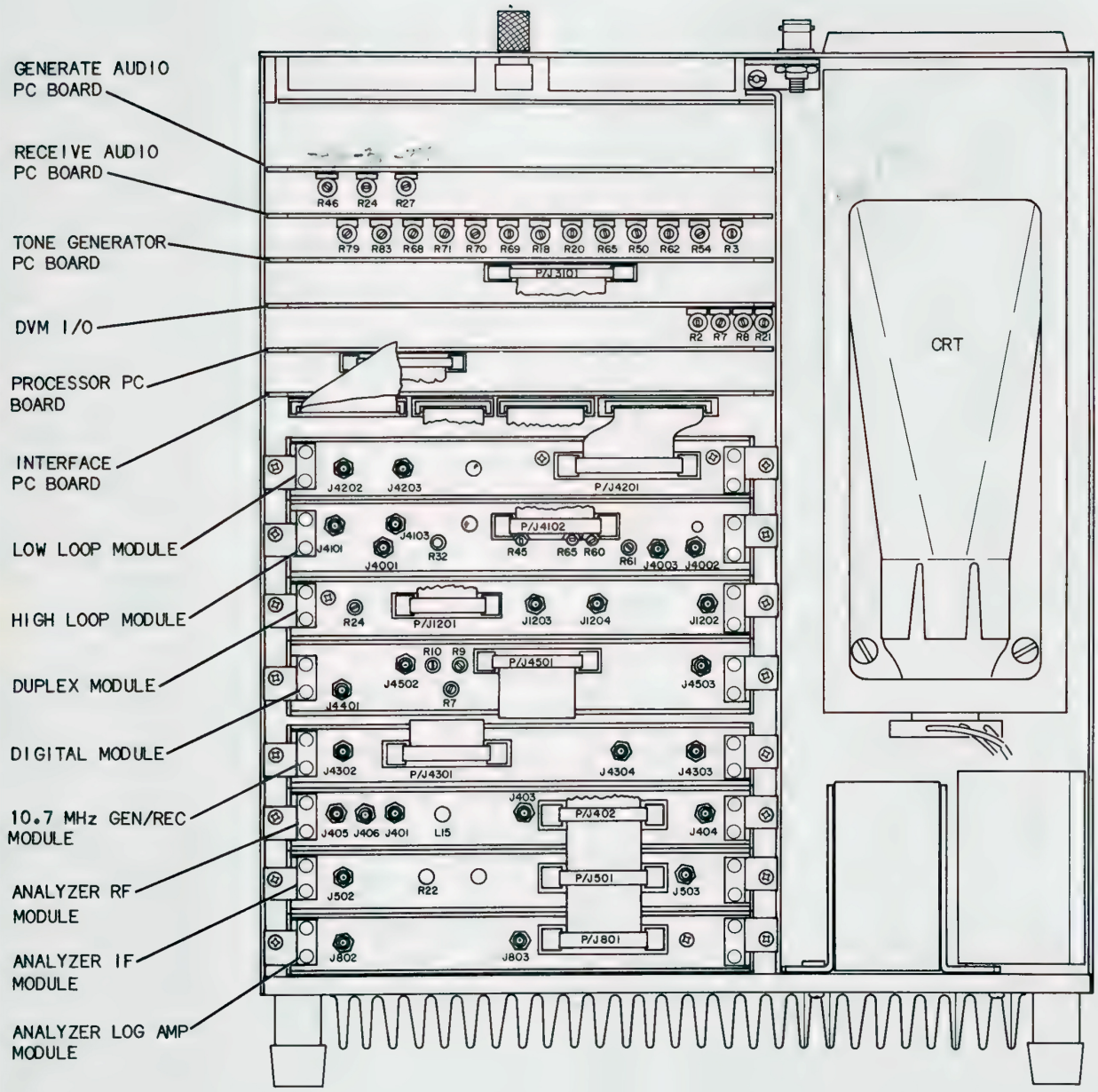
43. Set Signal Generator to -30 dBm. Adjust R812 on Analyzer Log Amp PC Board for a signal level of -30 dBm on CRT (31).

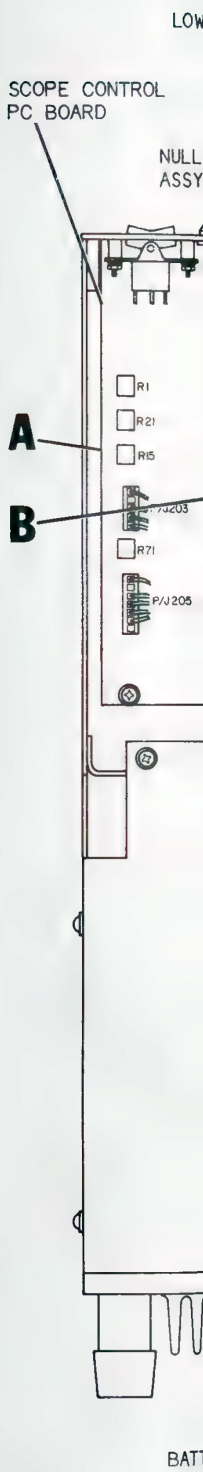
44. Repeat Steps 38 thru 43, as necessary to obtain required levels.

45. Set Signal Generator to -40 dBm. Rotate HORIZONTAL Sweep Selector Control (26) to "20 kHz/Div" Position and verify signal level is -40 dBm on CRT (31). Adjust R543 on Analyzer IF PC Board, as required, to obtain desired level.

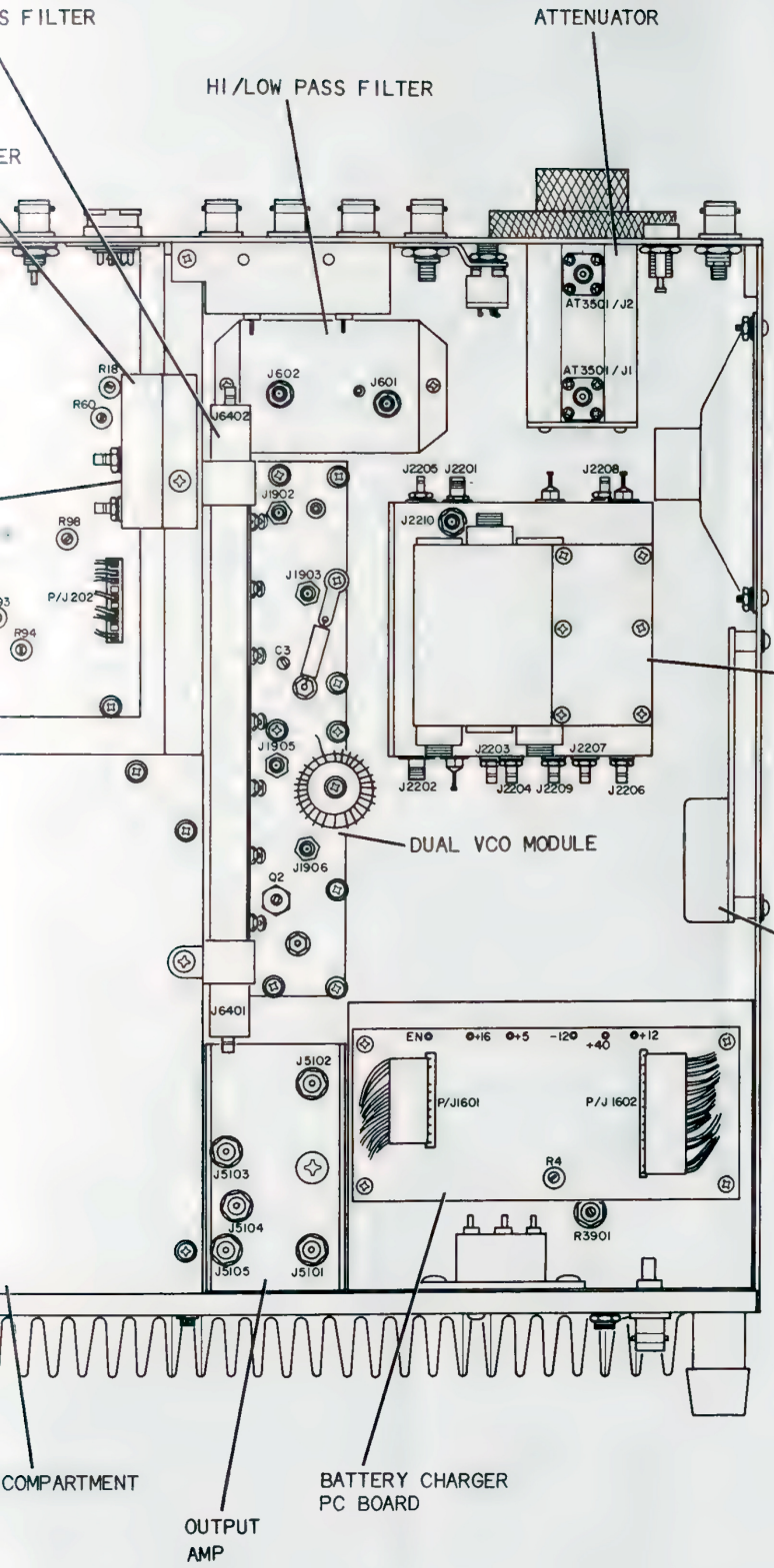
46. Place HORIZONTAL Sweep Selector Control (26) to "1 kHz/Div" Position and verify signal level on CRT (31) is -40 dBm. Adjust R559 on Analyzer IF PC Board, as necessary, to obtain desired level.

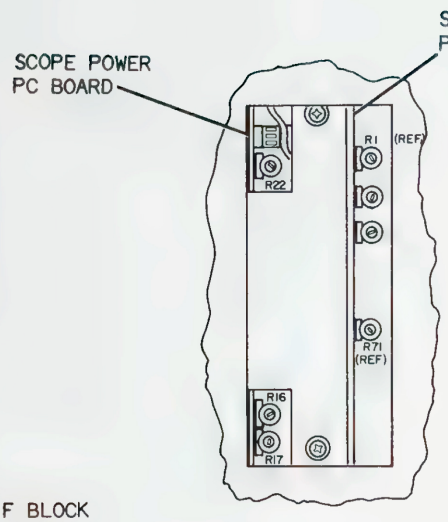
47. Disconnect test equipment, replace Analyzer Log Amp assembly and FM/AM-1200 cover.


GENERATE AUDIO PC BOARD
RECEIVE AUDIO PC BOARD
TONE GENERATOR PC BOARD
DVM I/O
PROCESSOR PC BOARD
INTERFACE PC BOARD
LOW LOOP MODULE
HIGH LOOP MODULE
DUPLEX MODULE
DIGITAL MODULE
10.7 MHz GEN/REC MODULE
ANALYZER RF MODULE
ANALYZER IF MODULE
ANALYZER LOG AMP MODULE
CRT
R46 R24 R27
R79 R83 R68 R71 R70 R69 R18 R20 R65 R50 R62 R54 R3
P/J3101
R2 R7 R8 R21
J4202 J4203 P/J4201
J4101 J4103 J4001 R32 P/J4102 R45 R65 R60 R61 J4003 J4002
R24 P/J1201 J1203 J1204 J1202
R10 R9 J4502 R7 P/J4501 J4503 J4401
J4302 P/J4301 J4304 J4303
J405 J406 J401 L15 J403 P/J402 J404
J502 R22 P/J501 J503
J802 J803 P/J801


LOW
SCOPE CONTROL PC BOARD
NULL ASSY
A
B
R1
R21
R15
R71
P/J205

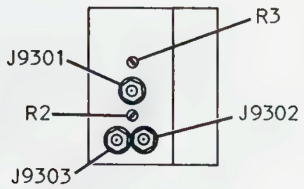
TOP VIEW





DETAIL **A**

Side View (Scope Power/ Scope Control PC Boards)



DETAIL **B**

Side View (Null Mixer Assy)

Figure 4-5 Location of Calibration Adjustments and Test Points

SECTION 5 - PREVENTIVE MAINTENANCE

5-1 GENERAL

Preventive maintenance on FM/AM-1200 test sets consists primarily of cleaning and visual inspection of internal/external components. External cleaning of the test set is recommended as often as necessary, depending on the environmental conditions to which the set is exposed. Internal cleaning should be performed on a more limited basis, preferably when the set is in a disassembled state for routine calibration, troubleshooting and/or repair. Test set disassembly for the sole purpose of internal cleaning is not recommended.

5-1-1 EXTERNAL CLEANING

1. Clean front panel and case with a soft lint-free cloth moistened with rubbing alcohol.

2. To remove tar or oil from outside case, safety solvent may be used.

CAUTION

DO NOT ALLOW SAFETY SOLVENT TO CONTACT FRONT PANEL CONTROL AREA. SOLVENT CAN CAUSE DAMAGE TO FRONT PANEL CONTROLS, MARKINGS ETC.

5-1-2 INTERNAL CLEANING AND INSPECTION

NOTE

The following procedures require external case to be removed from test set.

CAUTION

DELIBERATE MOVING (HOWEVER SLIGHT) OF DISCRETE COMPONENTS ON CIRCUIT BOARDS, ETC. SHOULD BE AVOIDED.

DO NOT OPEN INTERNAL MODULES FOR SOLE PURPOSES OF CLEANING.

1. Remove dust with hand-controlled dry air jet of 15 psi (1.054 kg/cm^2) and wipe internal chassis parts and frame with soft lint-free cloth moistened with alcohol.

1. (Continued)

WARNING

DO NOT USE COMPRESSED AIR IN EXCESS OF 15 PSI. USE EXTREME CARE WHEN USING COMPRESSED AIR IN THE VICINITY OF CRT, IN ORDER TO MINIMIZE POSSIBILITY OF CRT IMPLOSION. OBSERVE FOLLOWING PRECAUTIONS:

a. REMOVE ANY LARGE DIRT/DUST PARTICLES FROM CRT MANUALLY, AS OPPOSED TO USING COMPRESSED AIR.

b. DO NOT USE COMPRESSED AIR IN A DIRTY, CLUTTERED ENVIRONMENT. REMOVE ANY DEBRIS OR SMALL OBJECTS IN THE IMMEDIATE WORK AREA THAT MAY BECOME AIRBORNE DUE TO PRESSURIZED AIRFLOW.

c. IF POSSIBLE, USE AN AIR HOSE NOZZLE EQUIPPED WITH A SPRING LOADED ON/OFF VALVE, AS OPPOSED TO ONE THAT REMAINS OPEN OR CLOSED CONTINUOUSLY.

d. MAKE SURE COMPRESSED AIR HOSE IS FILTERED, TO PREVENT POSSIBLE OIL OR WATER DROPLETS FROM STRIKING CRT AT HIGH SPEEDS.

2. Inspect CHASSIS for:

a. Tightness of subassemblies and chassis mounted connectors.

b. Corrosion or damage to metal surfaces.

3. Inspect CAPACITORS for:

a. Loose mounting, deformities or obvious physical damage.

b. Leakage or corrosion around leads.

4. Inspect CONNECTORS for:

a. Loose or broken parts, cracked insulation and bad contacts. DO NOT disassemble connectors needlessly within test set.

5. Inspect POTENTIOMETER CONTROLS for:

a. Free rotation. If rotation feels rough, check control with an ohmmeter.

6. Inspect readily accessible PRINTED CIRCUIT BOARDS for:

a. Corrosion or damage to connectors.

6. (Continued)

   b. Damage to all mounted components including crystals and I.C.'s.

   c. Accumulation of dirt, dust or other foreign material.

7. Inspect RESISTORS for:

   a. Cracked, broken, charred or blistered bodies.

   b. Loose or corroded solder connections.

8. Inspect SEMICONDUCTORS for:

   a. Cracked, broken, charred or discolored bodies.

   b. Seals around leads being in place and in good condition.

9. Inspect TOGGLE SWITCHES for:

   a. Loose levers or terminals and switch body contact to frame.

   b. Bent or loose line switch contacts.

10. Inspect TRANSFORMER for:

    a. Signs of excessive heating.

    b. Broken or charred insulation and loose mounting hardware.

11. Inspect WIRING for:

    a. Broken or loose ends and connections.

    b. Proper dress relative to other chassis parts.

NOTE

All laced wiring should be tight with ends securely tied.

SECTION 6 - MECHANICAL ASSEMBLIES

6-1 GENERAL

This section contains "exploded view" drawings of all mechanical assemblies within the FM/AM-1200 except PC Boards. Pertinent notes for disassembly and/or reassembly are included as required with individual drawings.

These drawings are sequenced in the order they are discussed in Section 2 - Theory of Operation. (See index in paragraph 6-2.)

NOTE

The drawings in this section are not intended for use in ordering spare or replacement parts. For parts ordering information, see FM/AM-1200 Illustrated Parts Catalog.

6-2 ALPHABETICAL INDEX OF ASSEMBLY DRAWINGS

Title	Page No.
Analyzer IF Assembly	6-22
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Analyzer RF Assembly	6-21
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Digital Assembly	6-9
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Duplex Assembly	6-20
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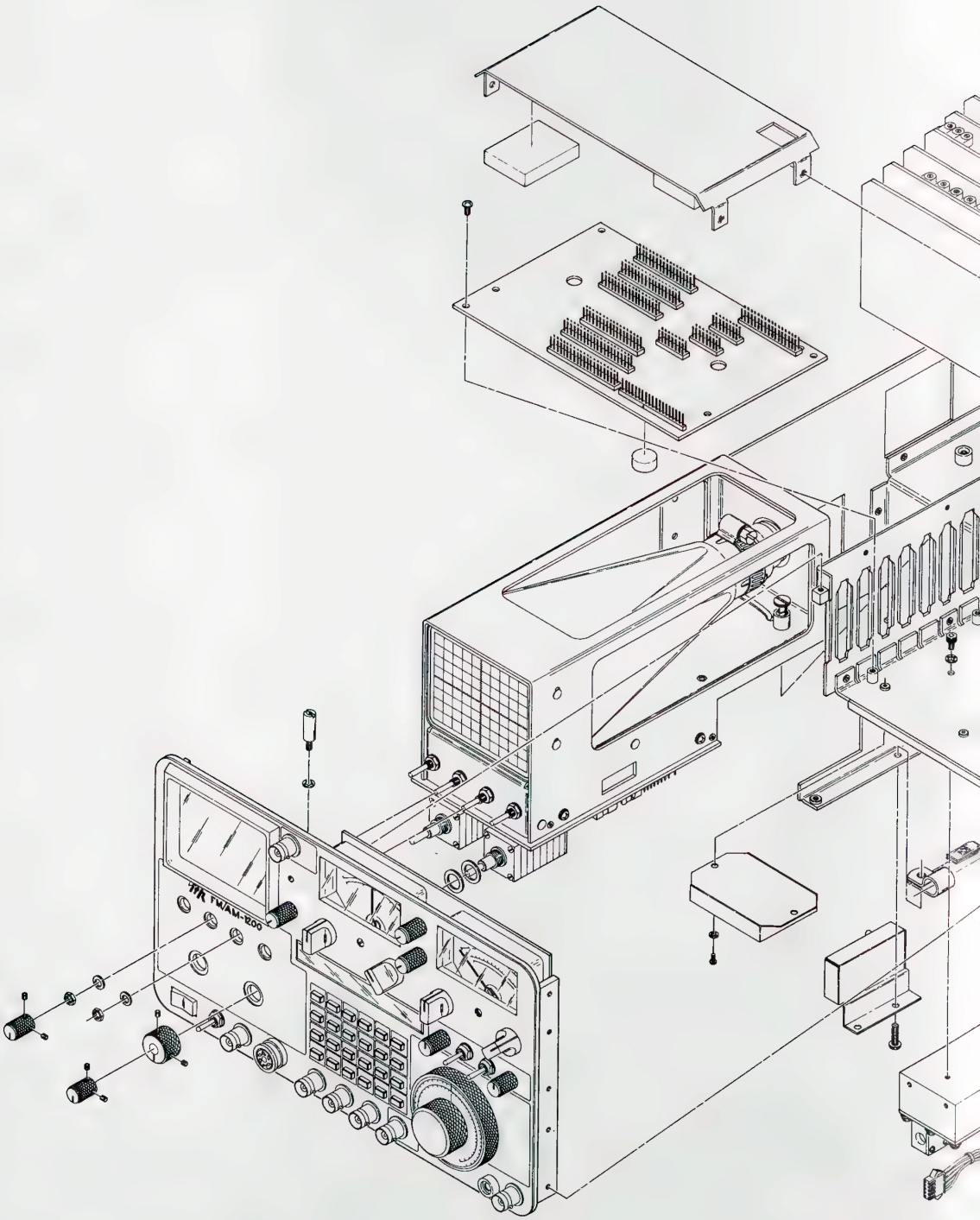
Null Mixer Assembly	6-17
Output Amplifier Assembly	6-19
Power Supply Assembly	6-8
Rear Panel Assembly	6-7
Scope Power and Control Assembly	6-24
10.7 MHz Gen/Rec Assembly	6-11


TWAM-200

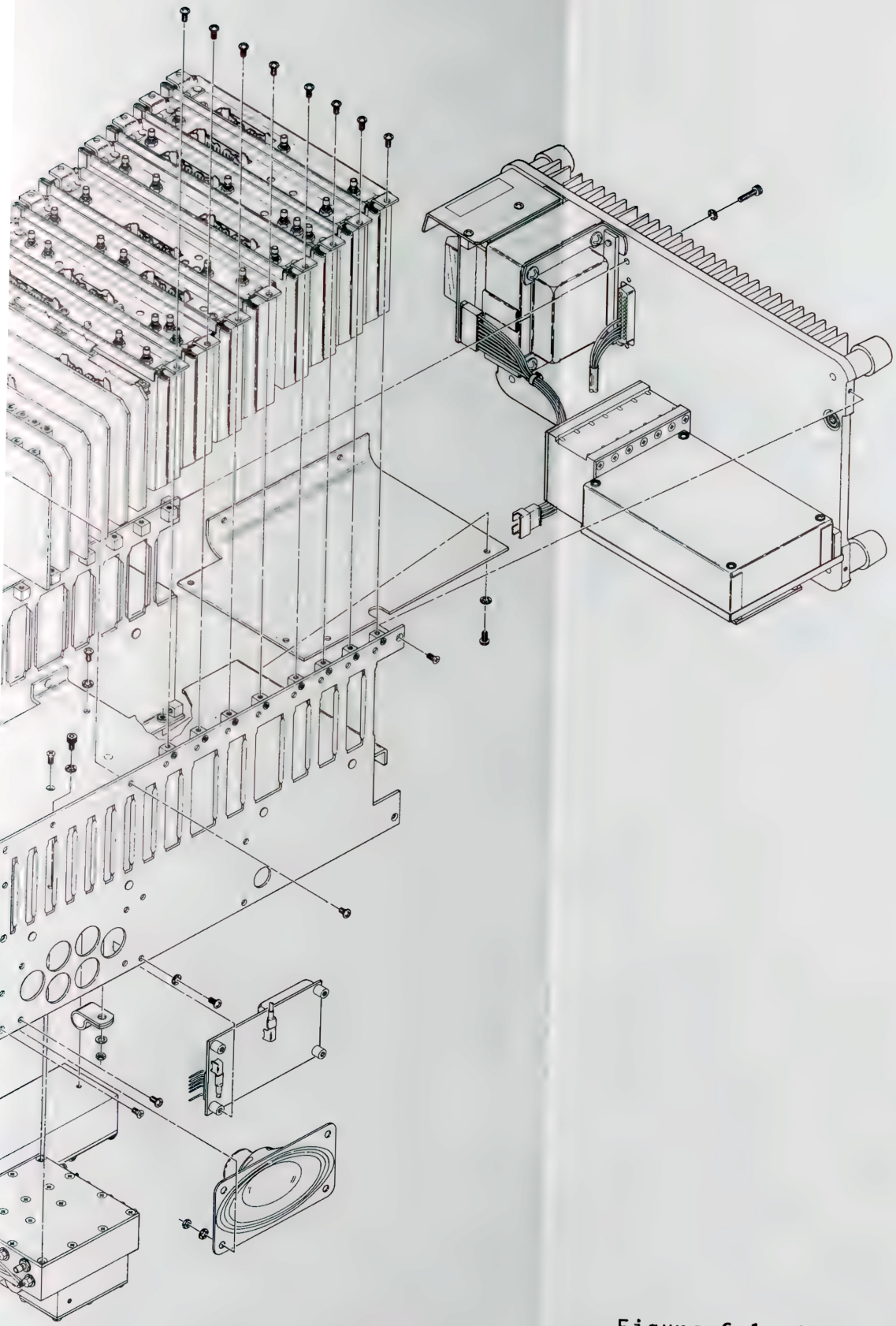
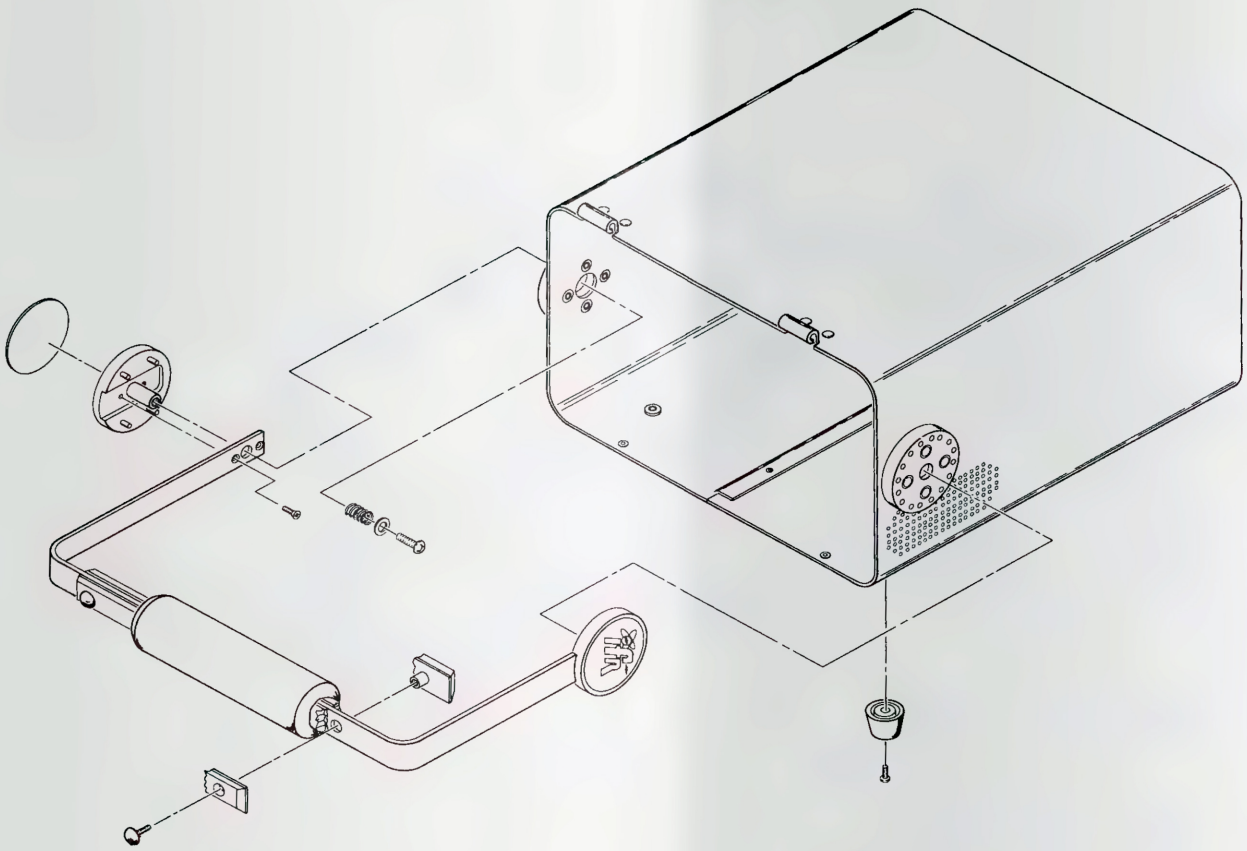
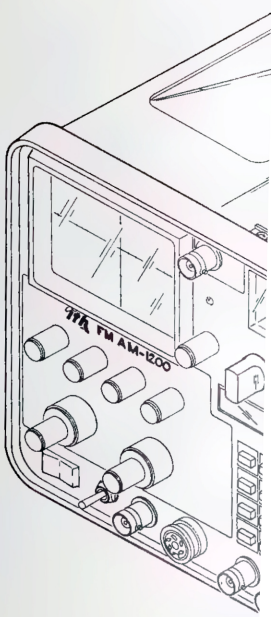


Figure 6-1 Composite Assembly





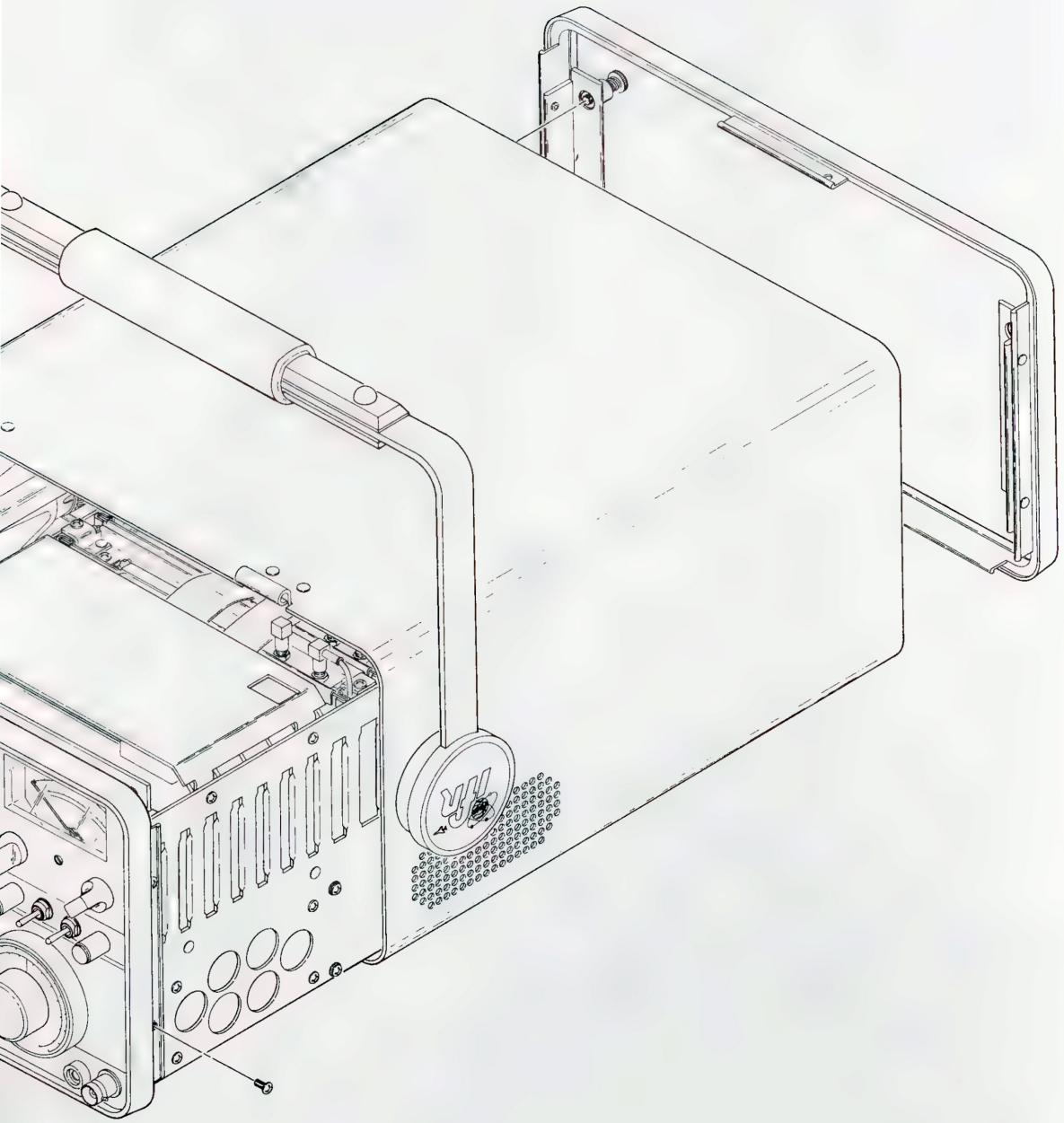


Figure 6-2 Case Assembly

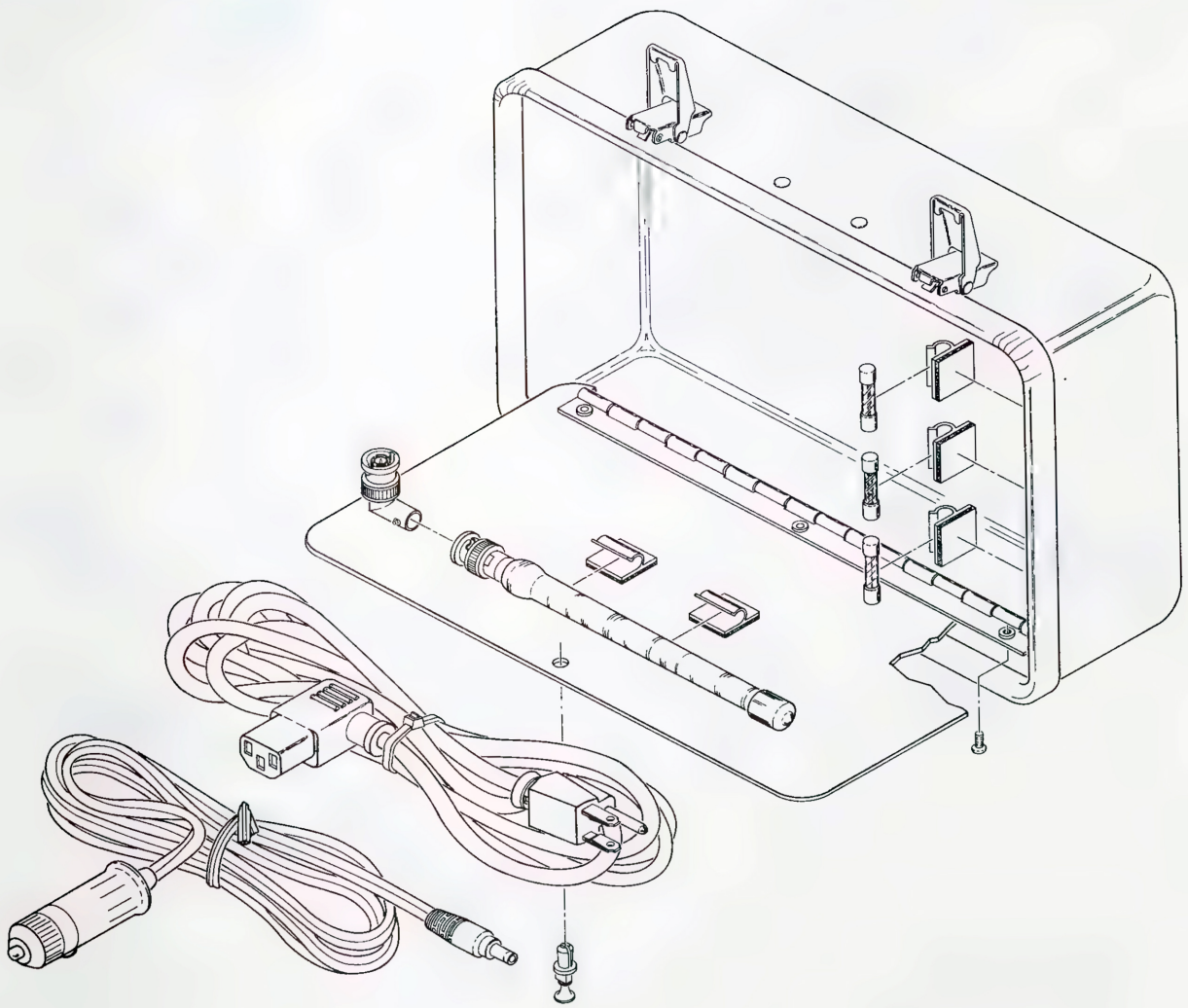


Figure 6-3 Lid Assembly

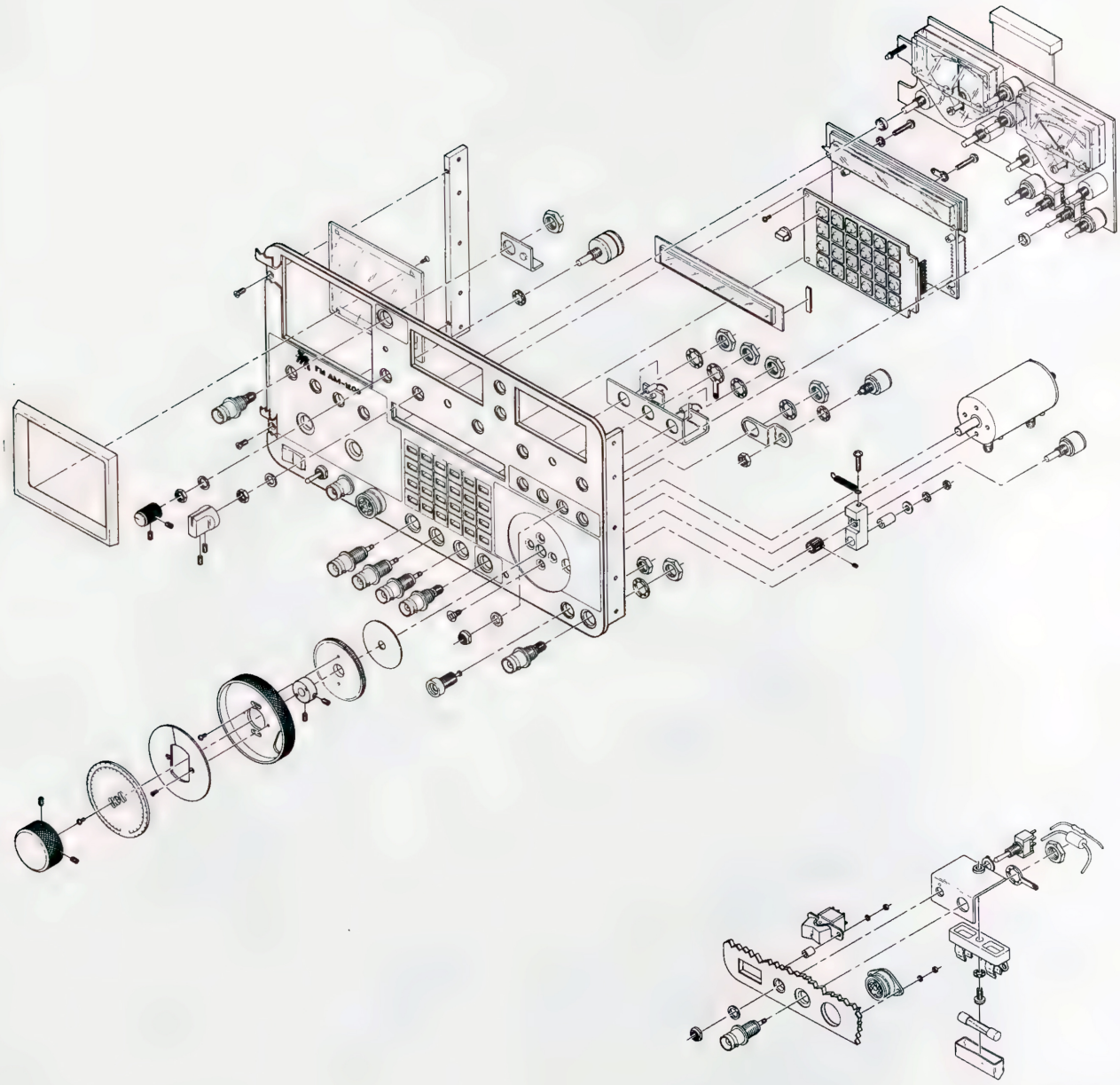


Figure 6-4 Front Panel Assembly

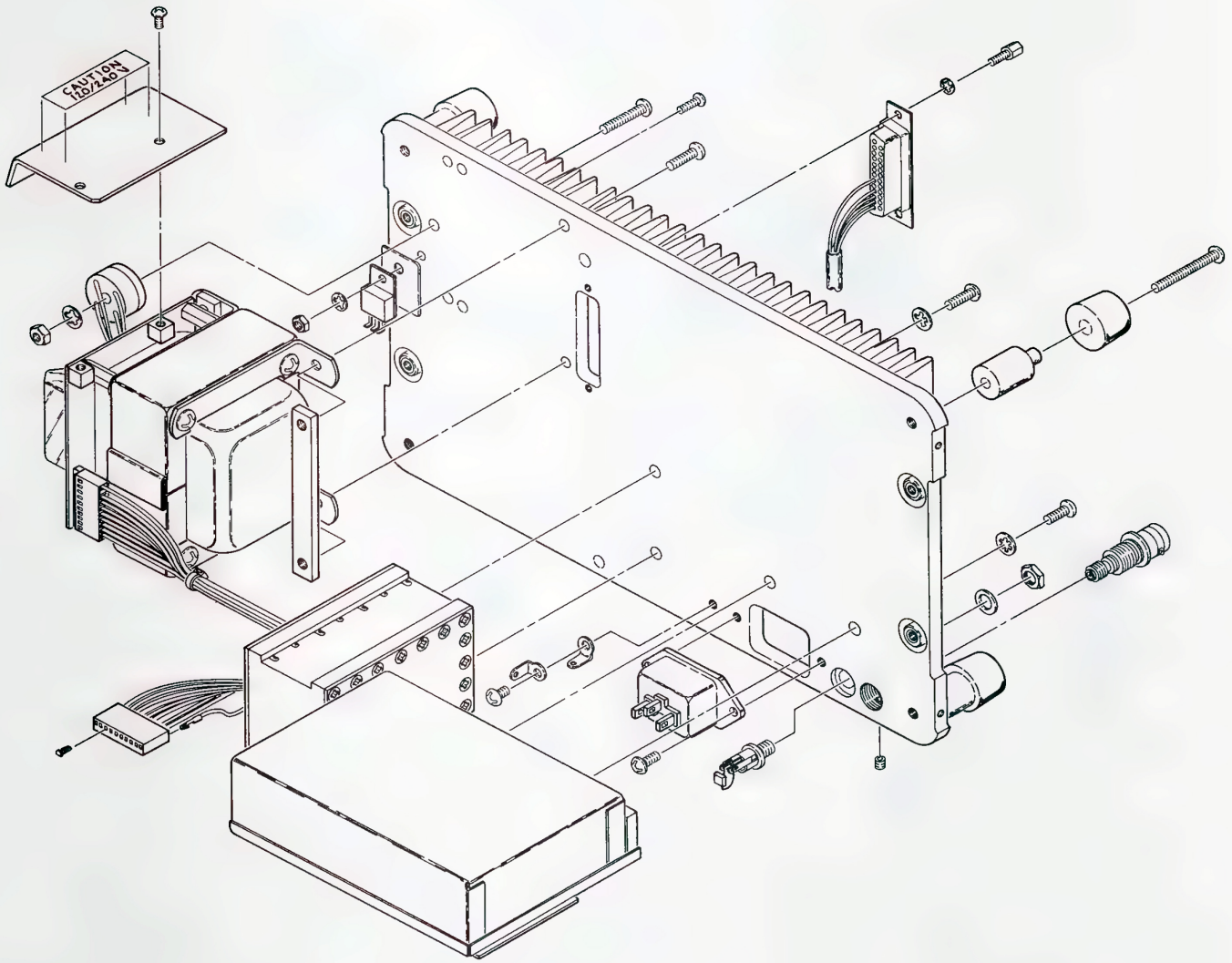


Figure 6-5 Rear Panel Assembly

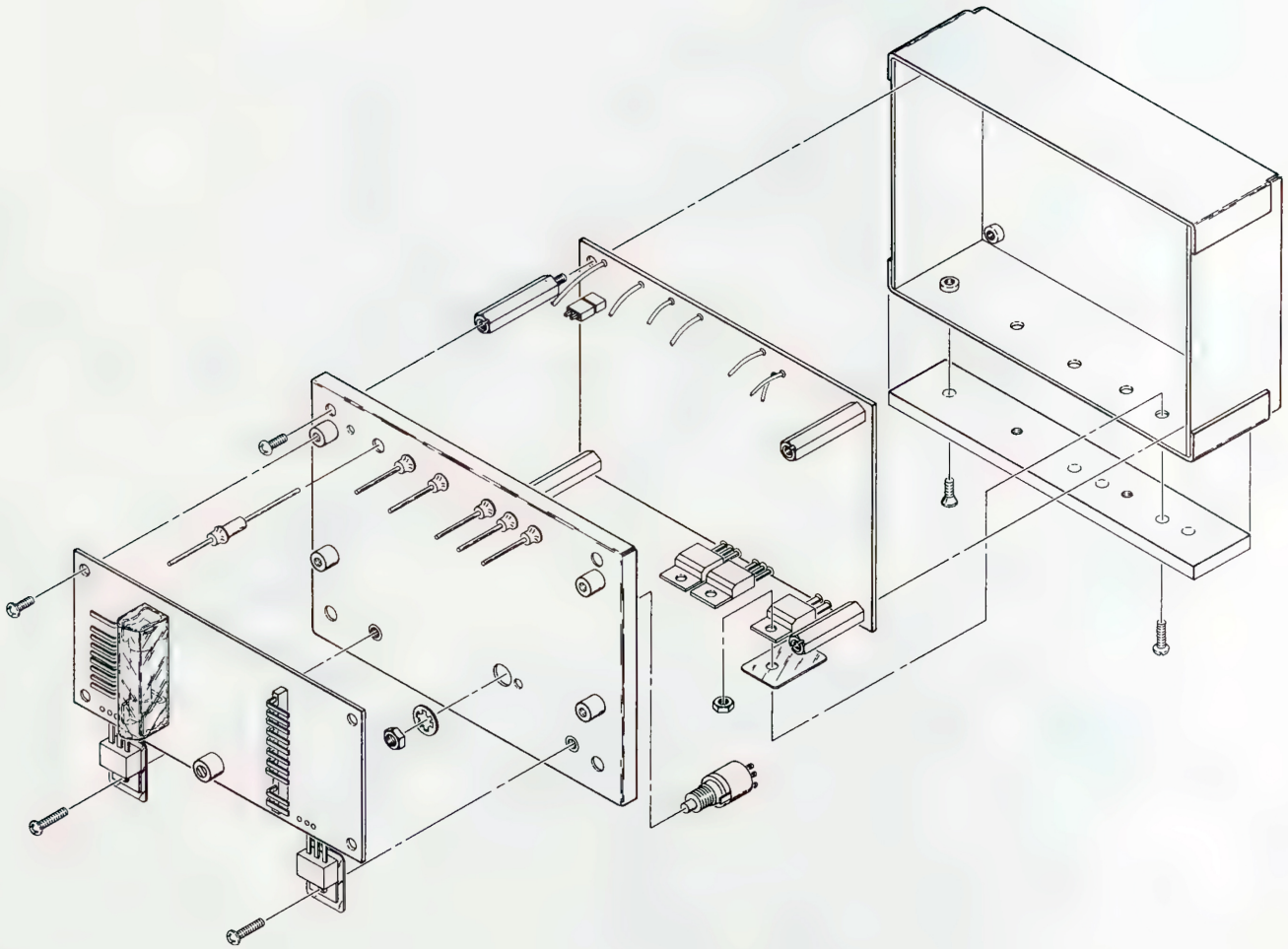


Figure 6-6 Power Supply Assembly

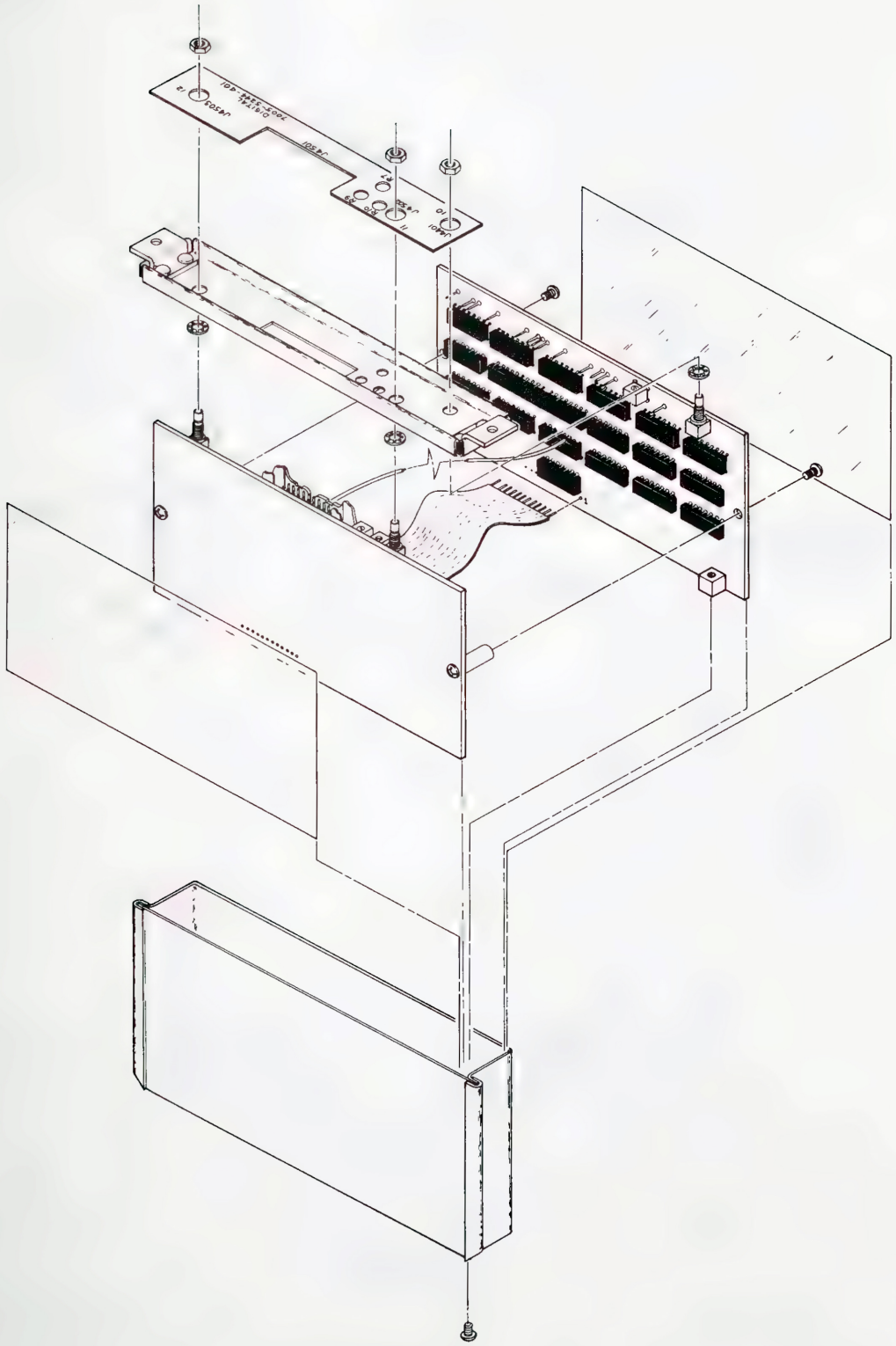


Figure 6-7 Digital Assembly

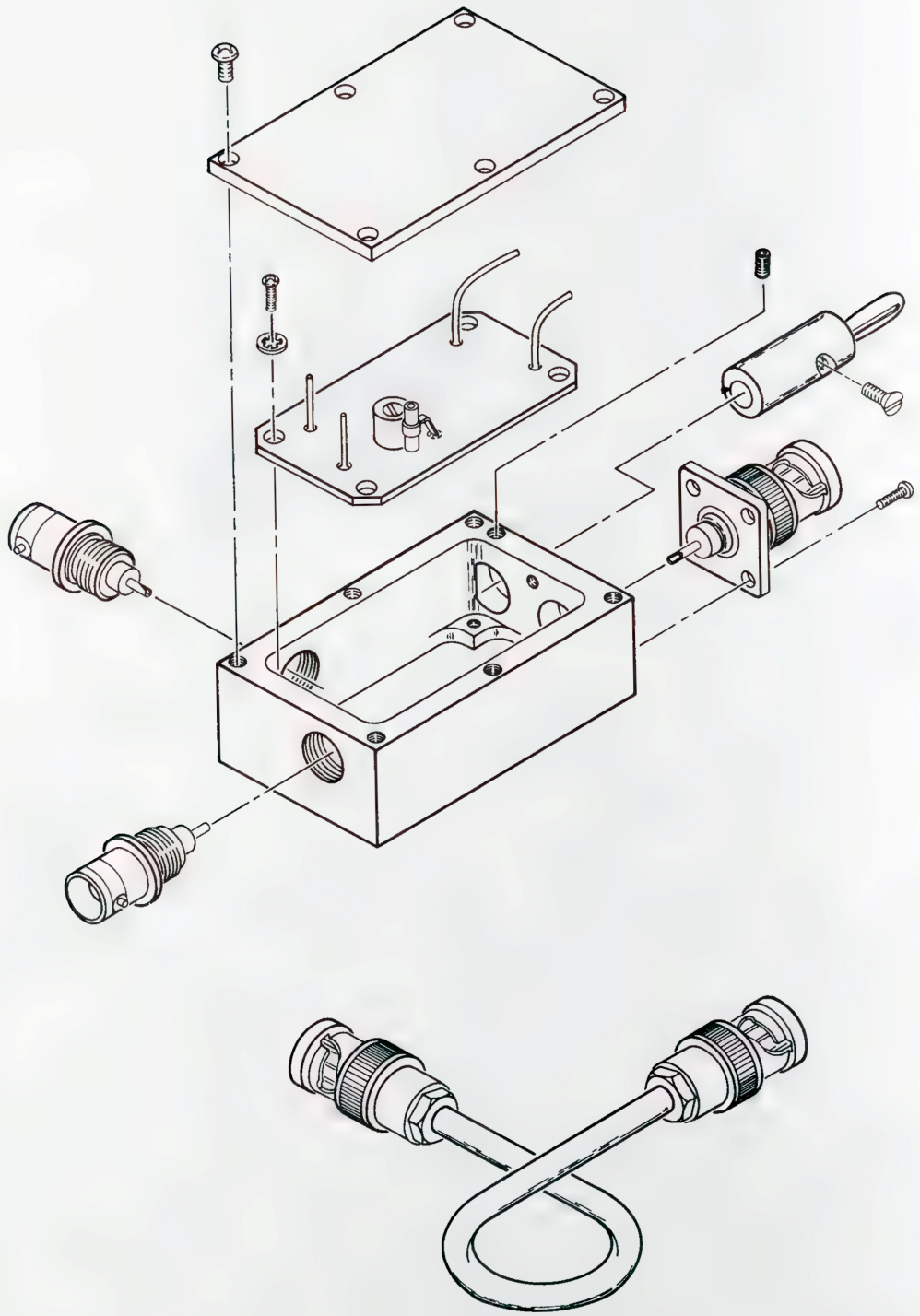


Figure 6-8 Generate Amplifier Assembly

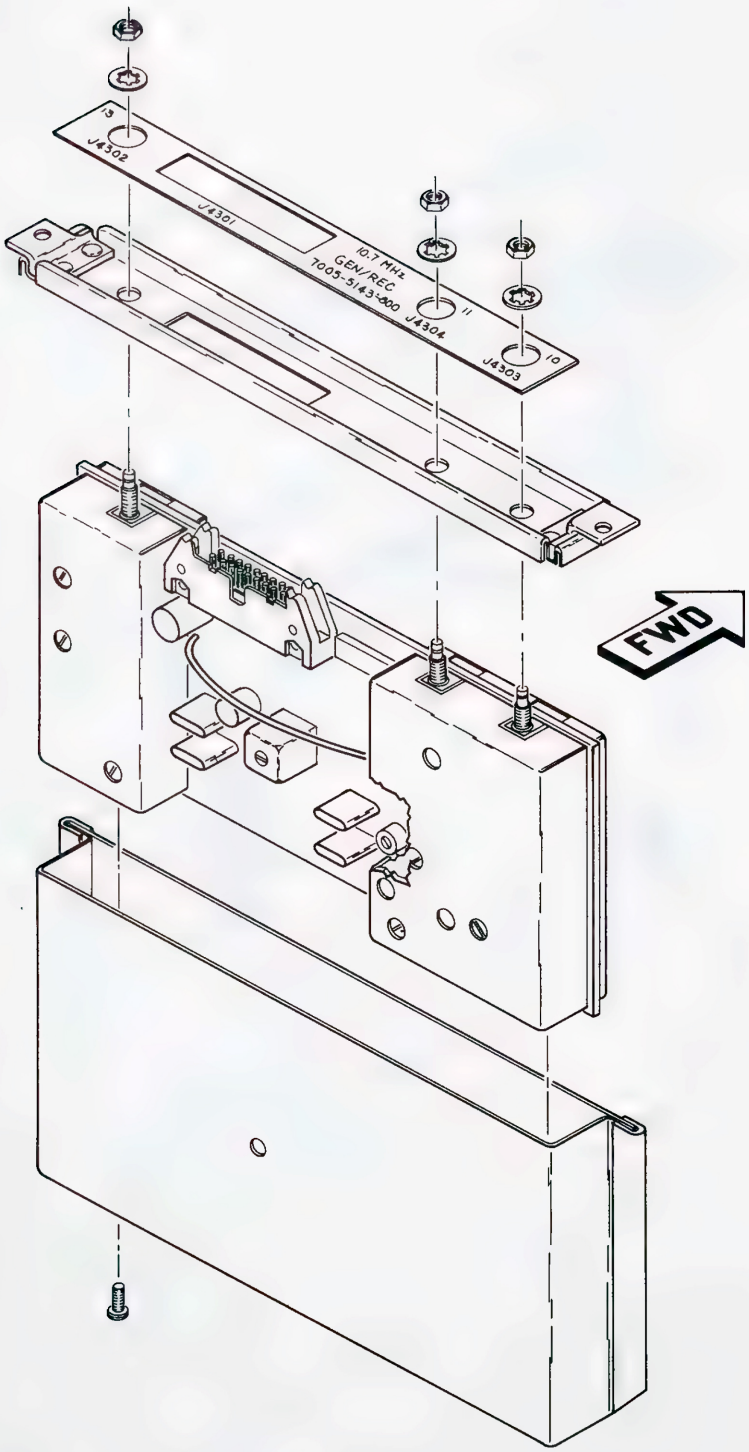


Figure 6-9 10.7 MHz Gen/Rec Assembly

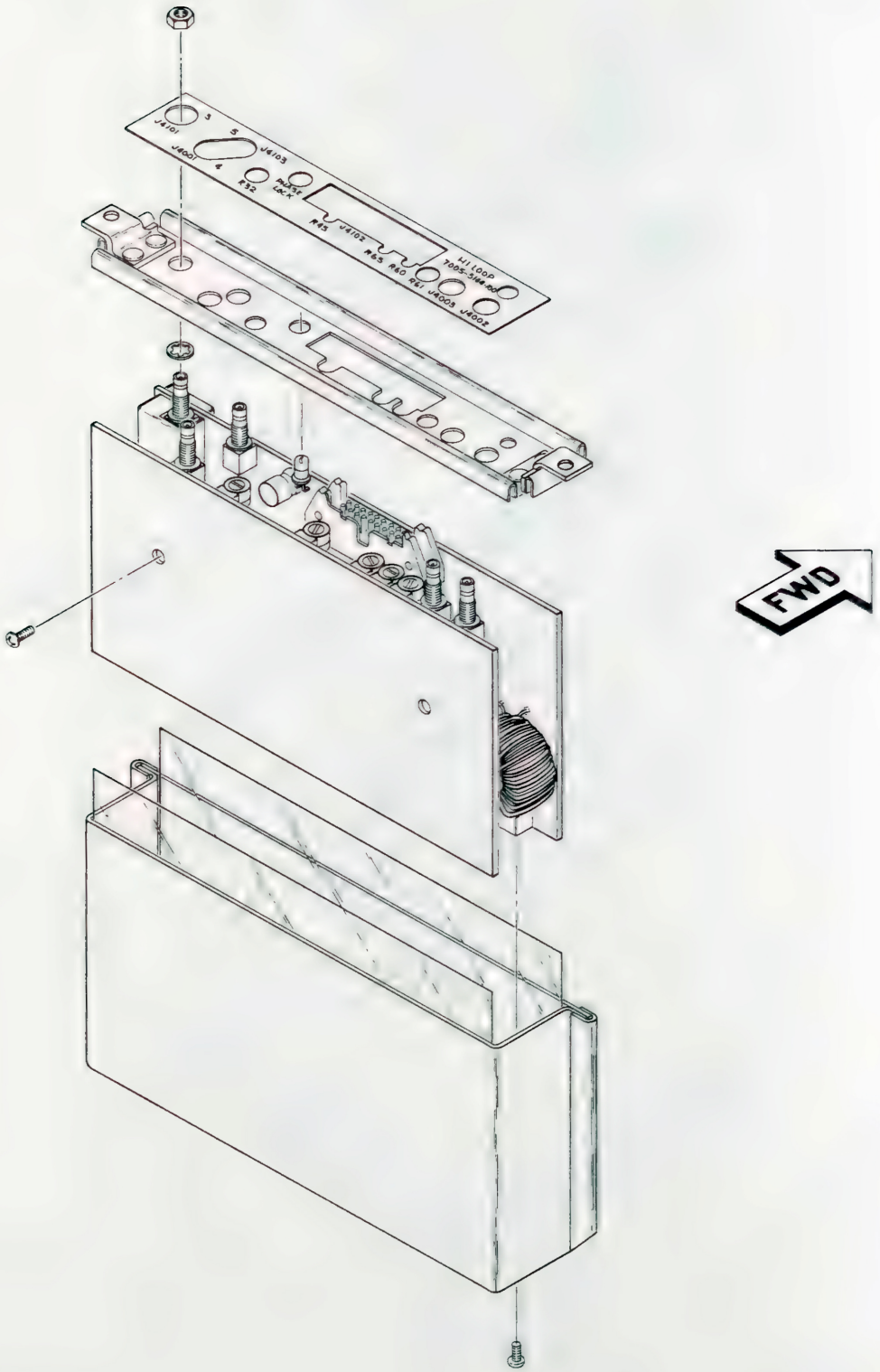


Figure 6-10 High Loop Assembly

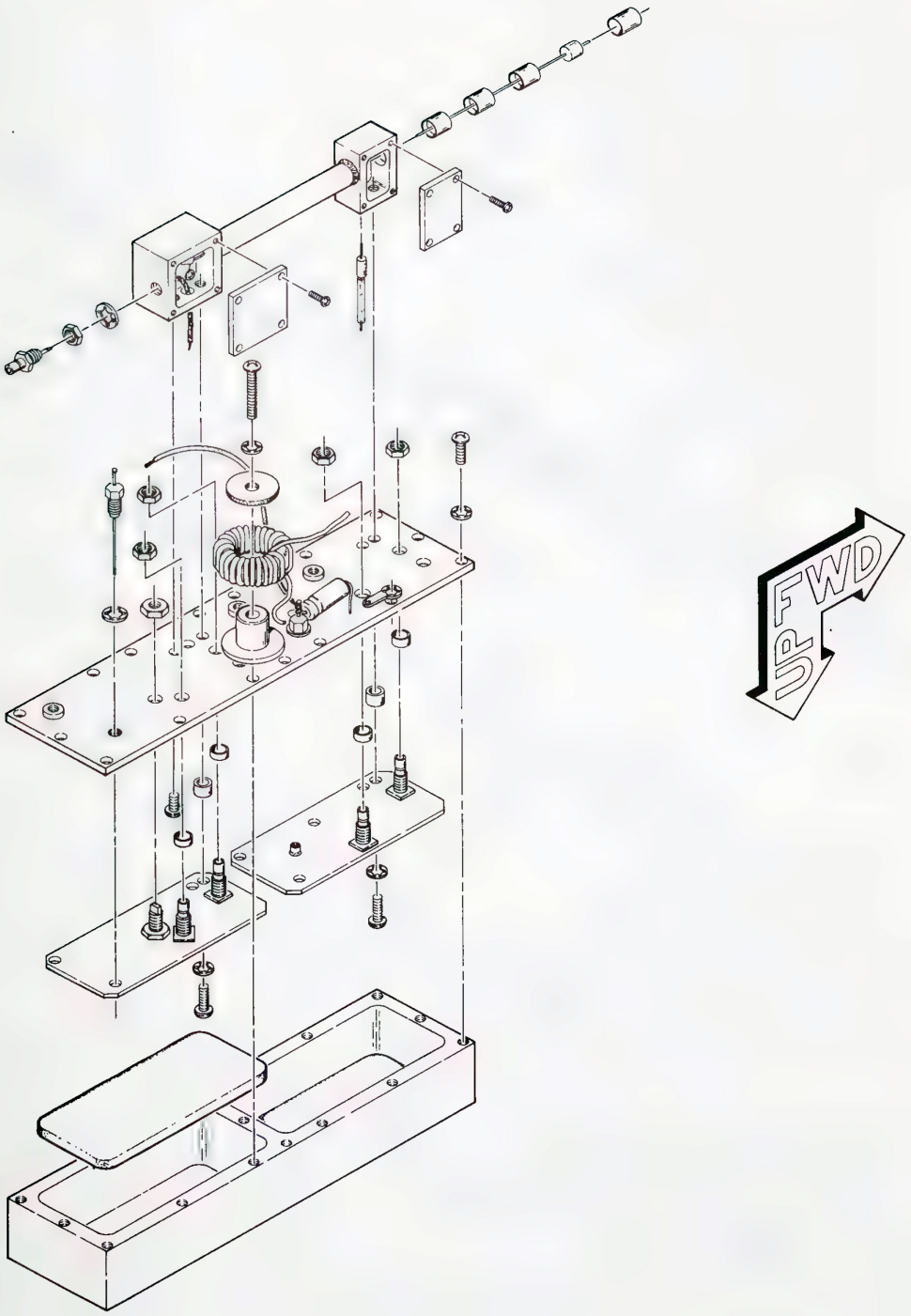


Figure 6-11 Dual VCO Assembly

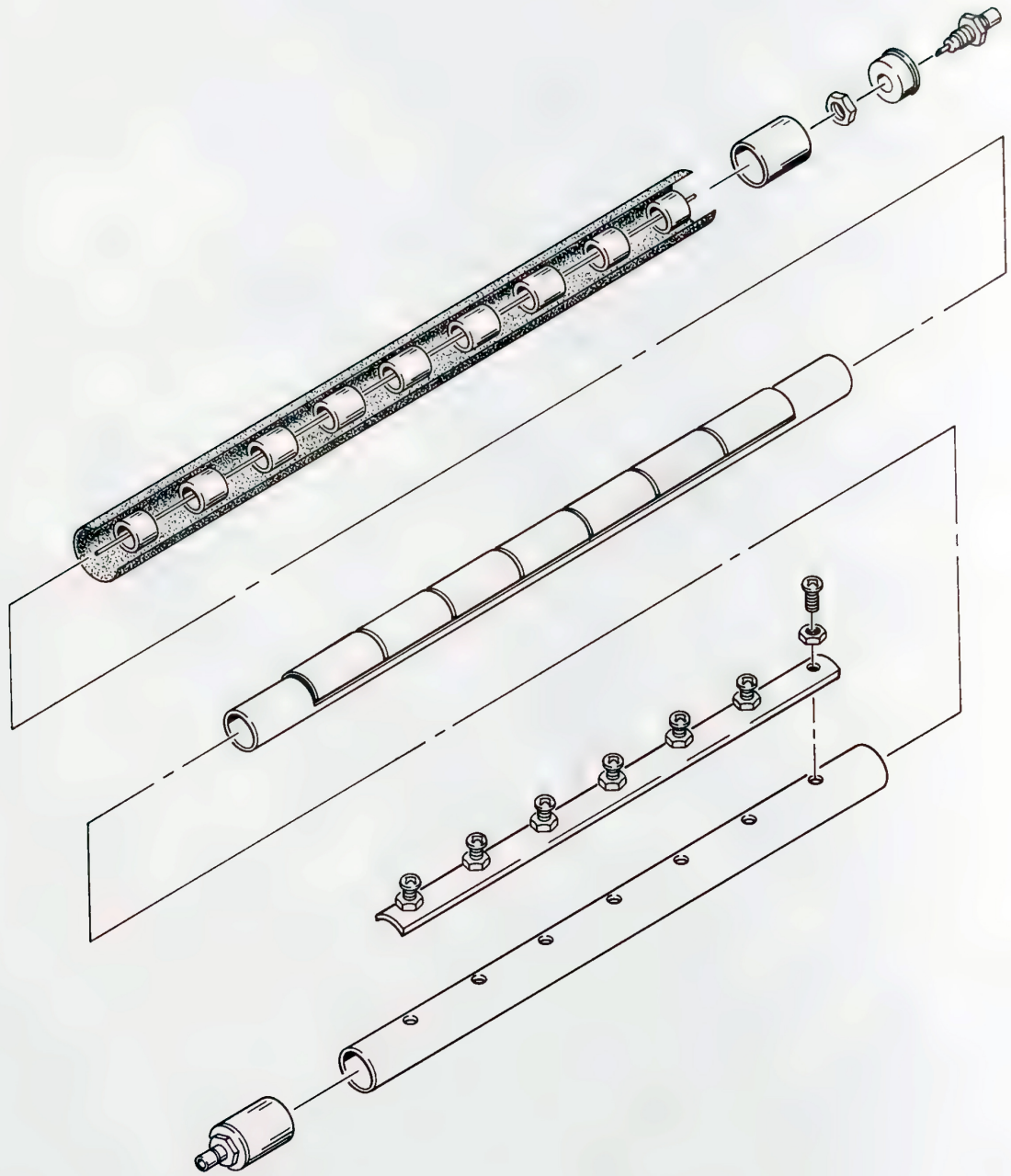


Figure 6-12 Low Pass Filter Assembly

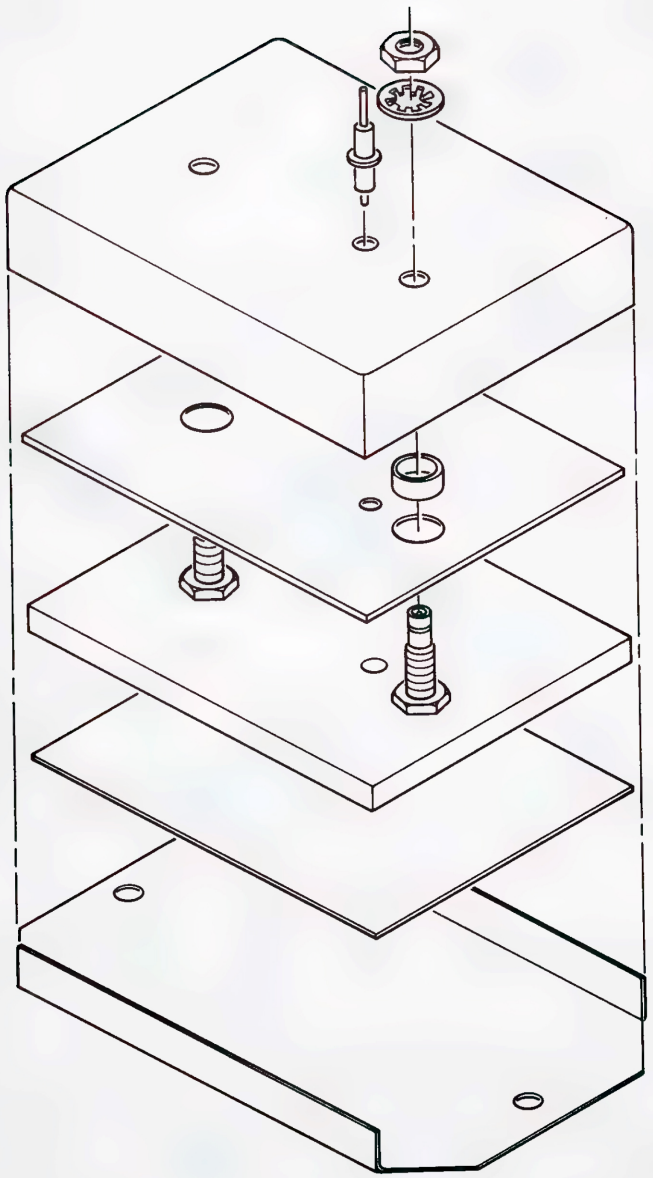


Figure 6-13 High-Low Pass Filter Assembly

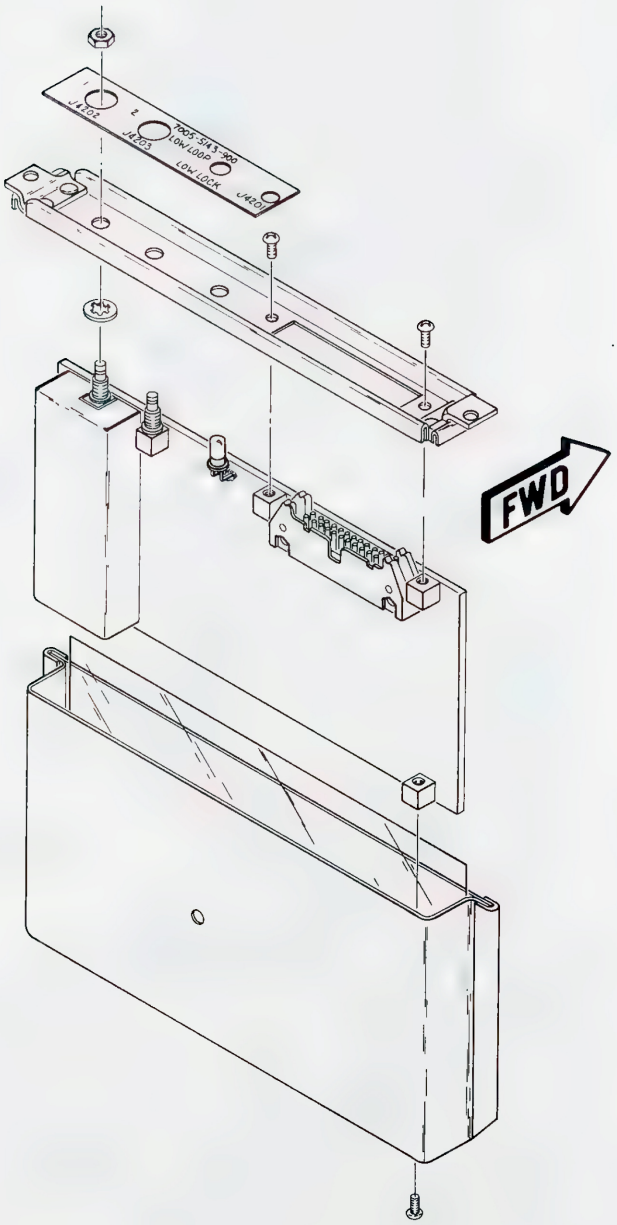


Figure 6-14 Low Loop Assembly

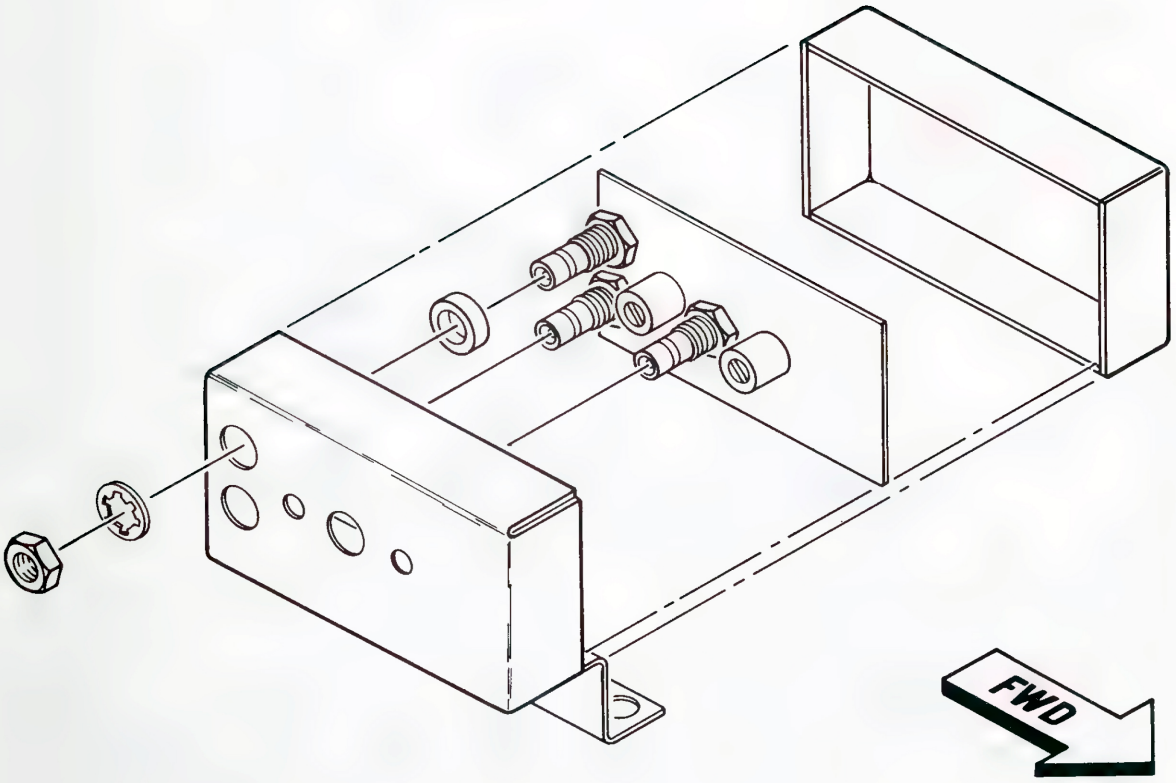


Figure 6-15 Null Mixer Assembly

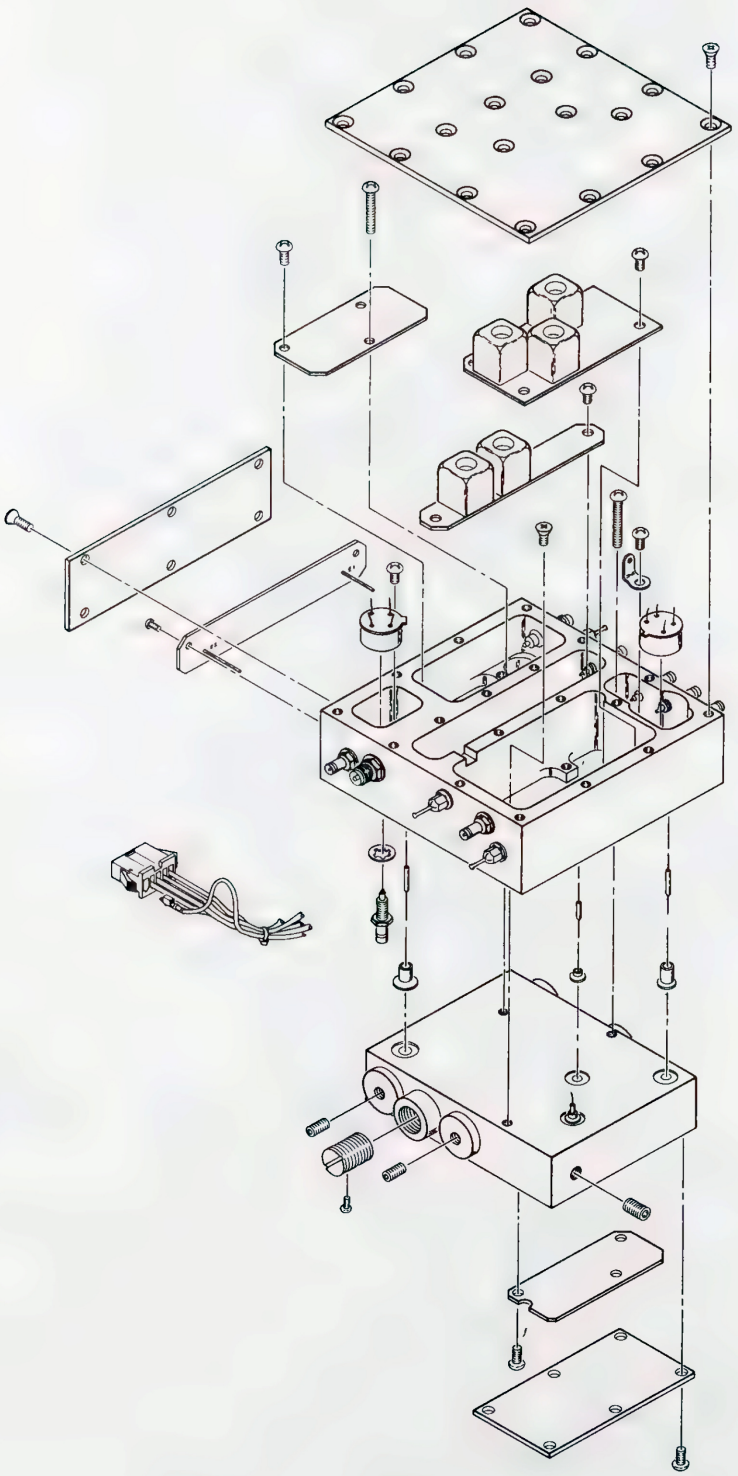


Figure 6-16 IF Block Assembly

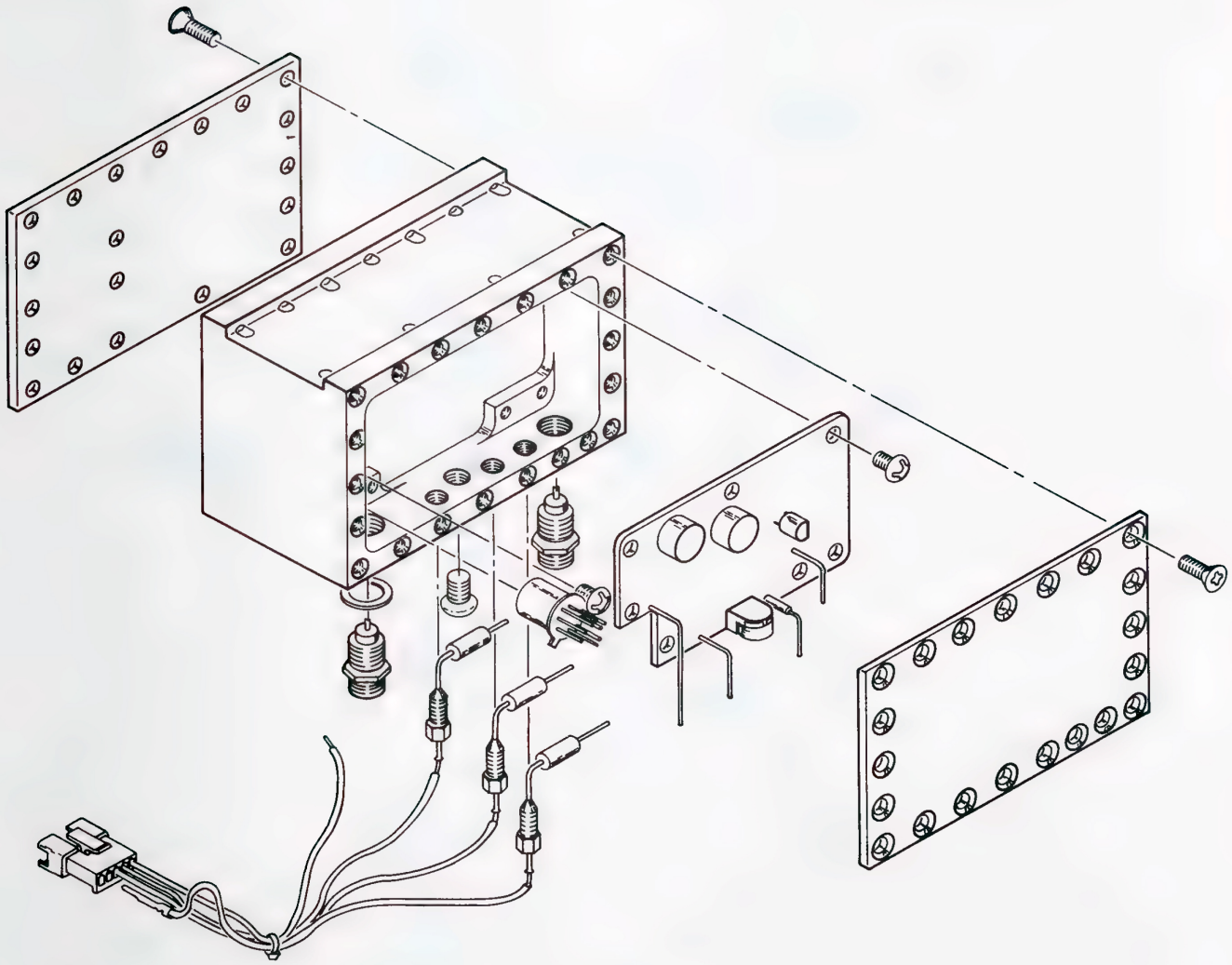


Figure 6-17 Output Amplifier Assembly

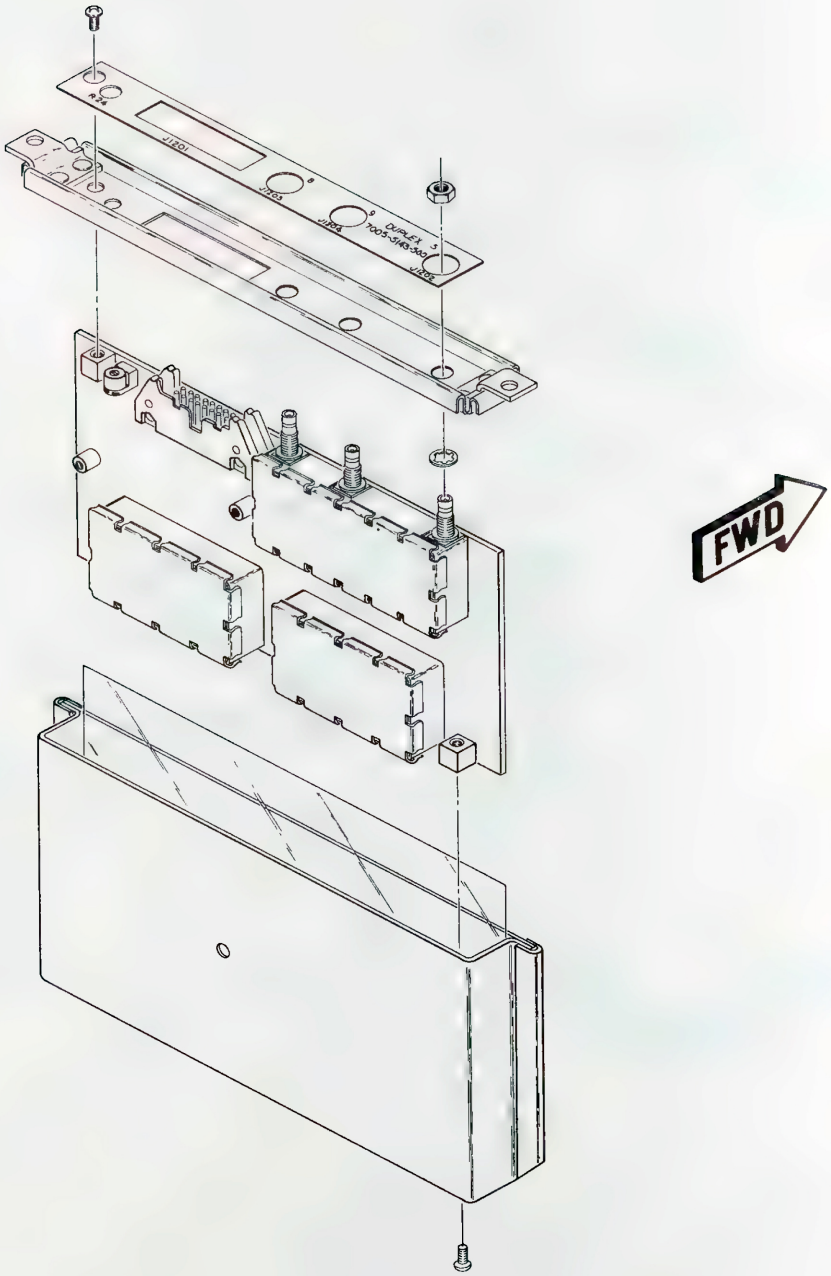


Figure 6-18 Duplex Module Assembly

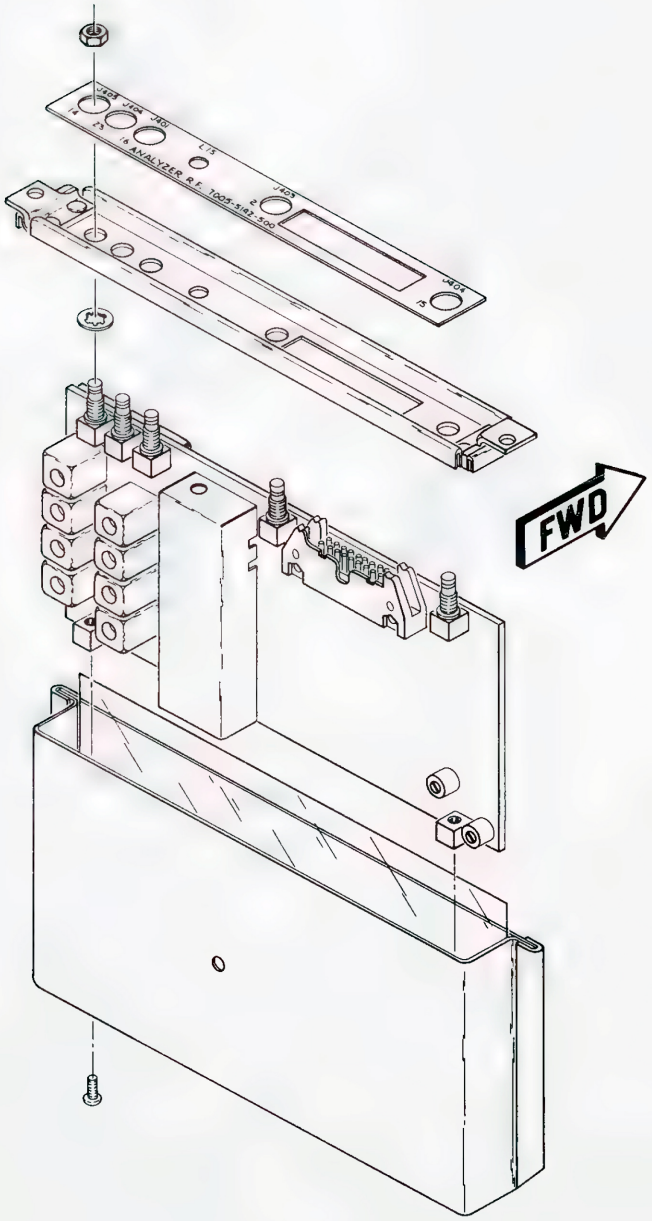


Figure 6-19 Analyzer RF Assembly

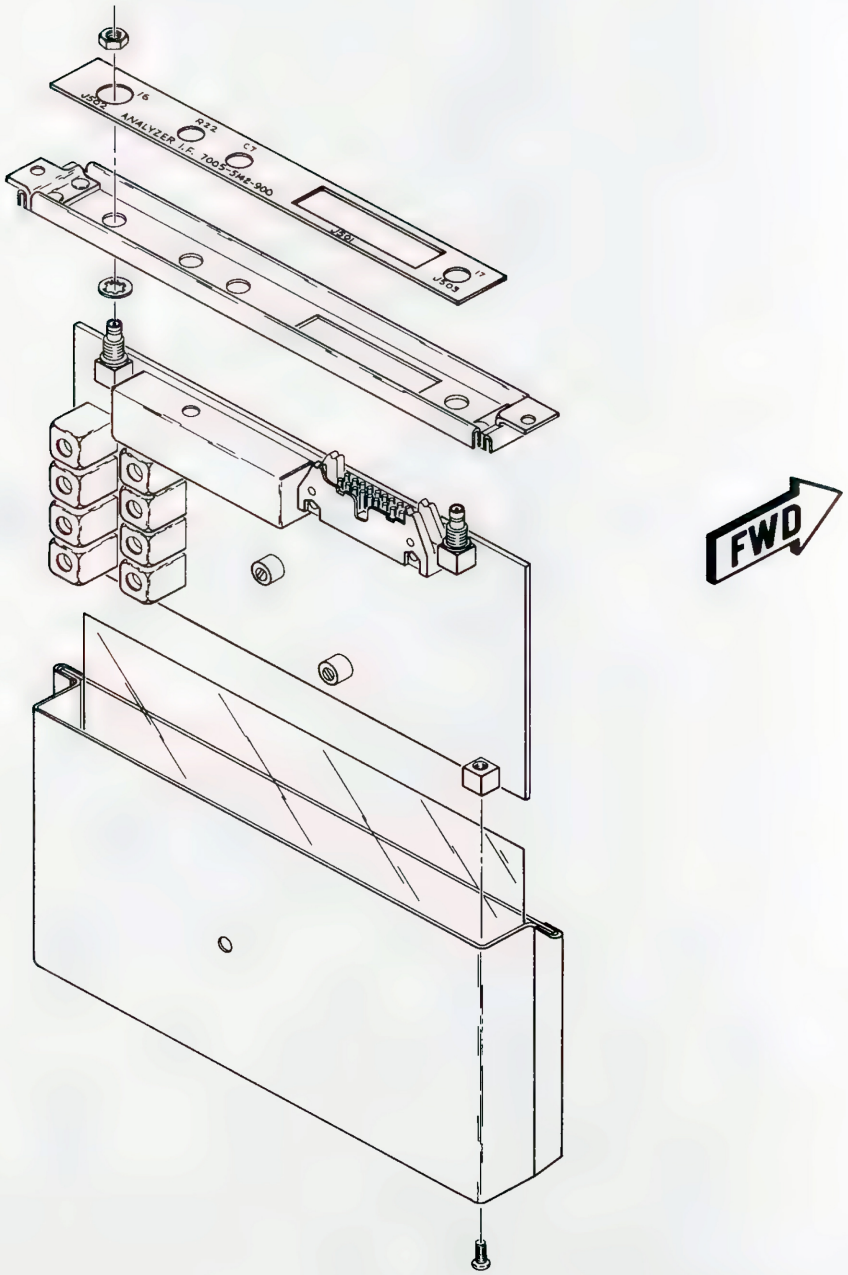


Figure 6-20 Analyzer IF Assembly

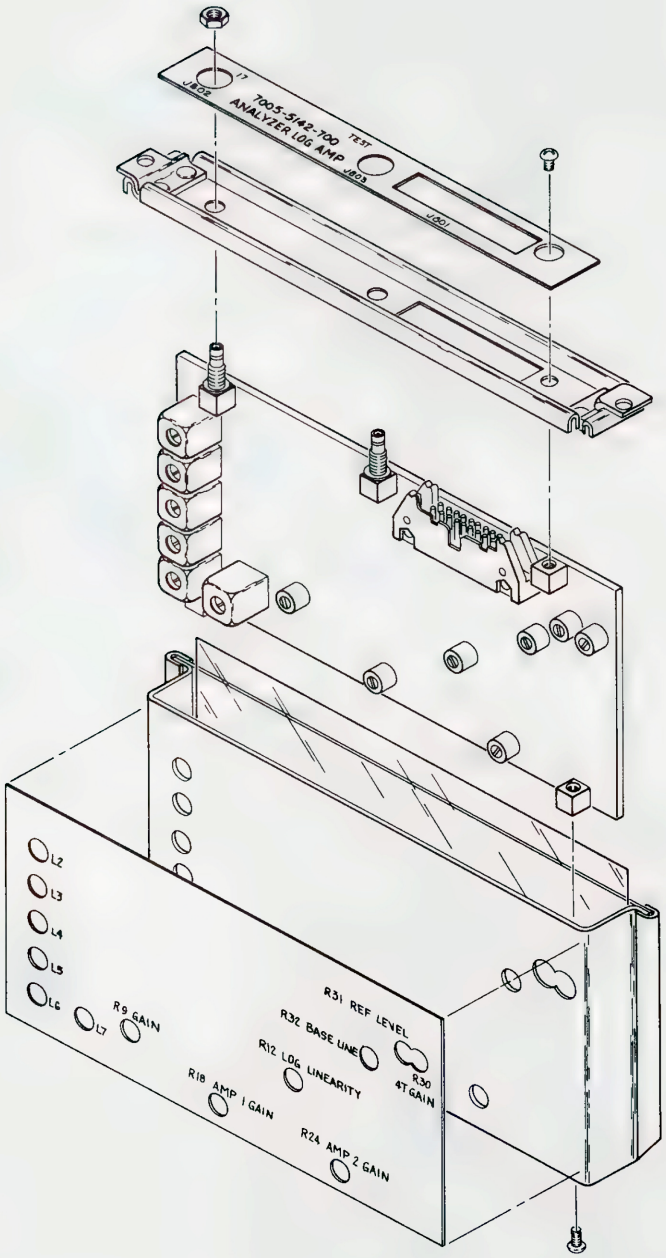
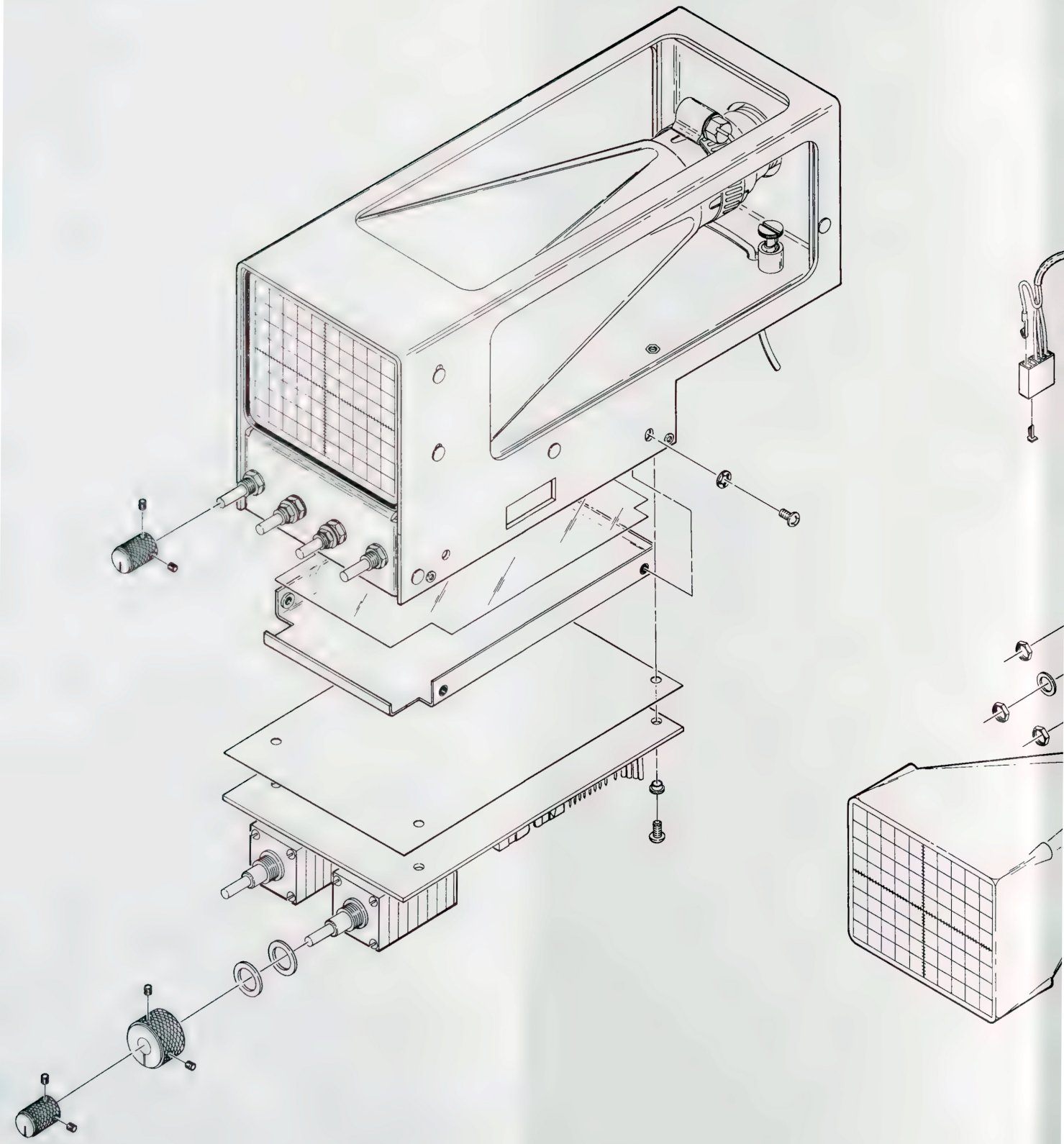

7005-5142-700
ANALYZER LOG AMP
TEST
J803
J801
J802
L2
L3
L4
L5
L6
L7
R9 GAIN
R31 REF LEVEL
R32 BASE LINE
R12 LOG LINEARITY
R30
4T GAIN
R18 AMP 1 GAIN
R24 AMP 2 GAIN

Figure 6-21 Analyzer Log Amp Assembly



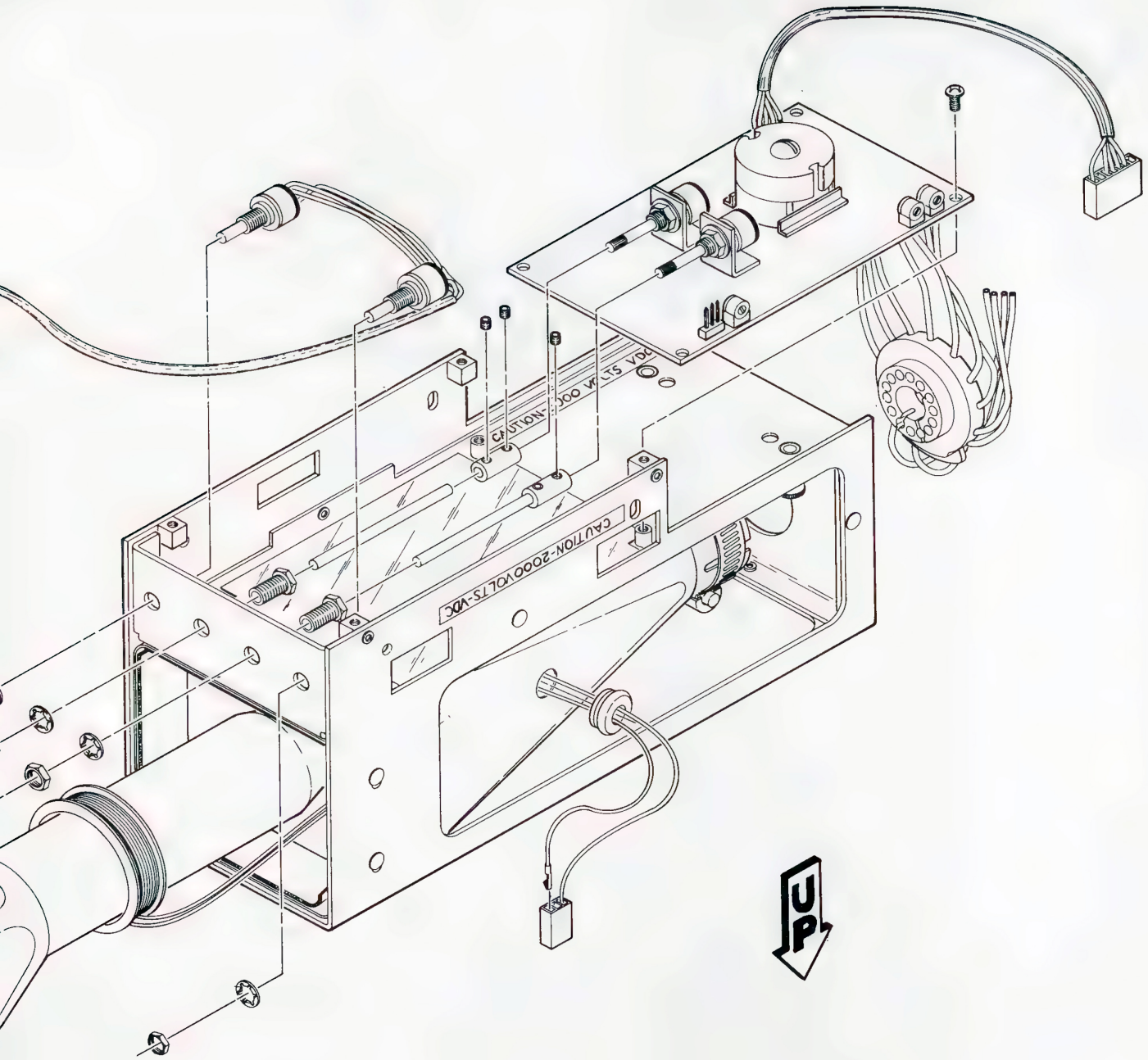


Figure 6-22 Scope Power and Control Assembly

SECTION 7 - PC BOARDS AND SCHEMATICS

7-1 GENERAL

This section contains component layout drawings for all PC Board assemblies, interconnect diagrams, circuit schematics, waveforms and charts reflecting voltage levels keyed to test points. These drawings are sequenced in the order they are discussed in Section 2 (Theory of Operation). An alphabetical index of all drawings for each module is contained in paragraph 7-3.

7-2 HOW TO USE SCHEMATICS

7-2 HOW TO USE SCHEMATICS

To trace coaxial cable conductors from one schematic to another follow the procedures outlined in paragraph 7-2-1, and to trace conductors for multiple pin connectors refer to paragraph 7-2-2.

7-2-1 Coaxial Cables

a. Locate desired module on Coaxial Cable Interconnect Drawing.

b. Locate desired coaxial cable on Interconnect Drawing. (Connectors are identified by reference designators.)

c. Follow coaxial cable on Interconnect Drawing to locate opposite end of conductor. Note cable reference designator and module of cables destination.

d. Locate schematic of desired module on index of circuit schematics in parapraph 7-3.

e. Locate reference designator of coaxial connector and continue tracing circuit.

7-2-2 Multiple Pin Connectors

a. Locate desired module on Interconnect drawing.

b. Locate desired multiple pin connector on Interconnect Drawing. Note reference designator of the mating connector.

c. Note module or wire harness on which the connector is mounted or grouped.

d. Locate schematic of desired module on index of circuit schematics in paragraph 7-3.

e. Using module schematic, locate reference designator of connector and corresponding pin number. Continue tracing circuit.

7-3 ALPHABETICAL INDEX OF INTERCONNECT DIAGRAMS AND CIRCUIT SCHEMATICS

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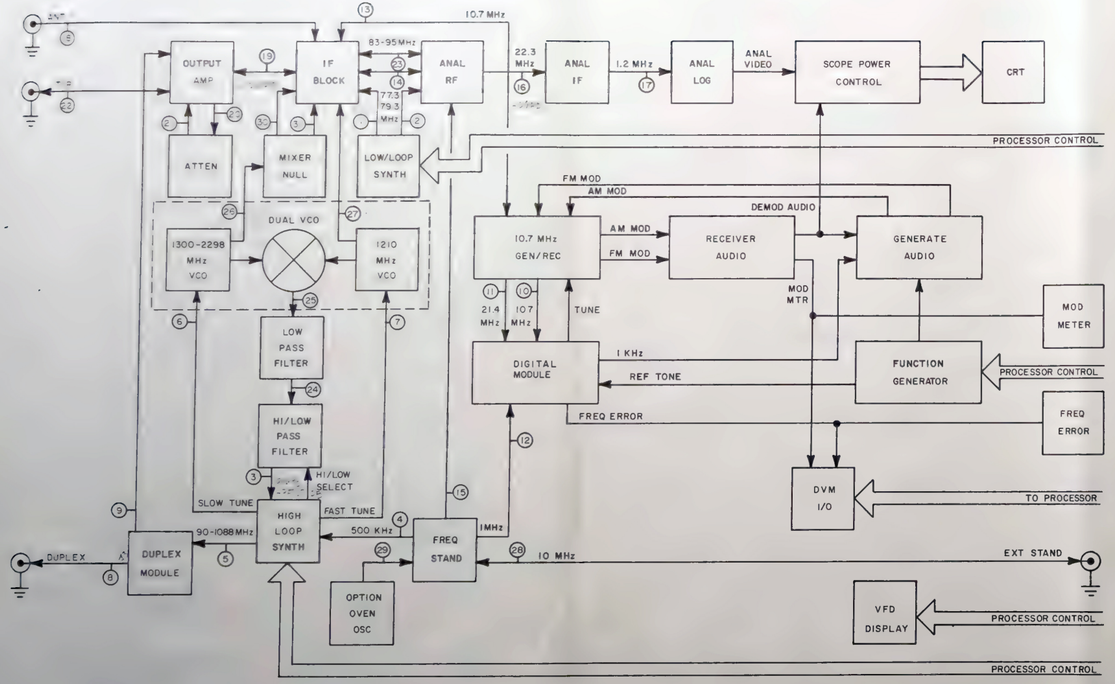
Scope Power and Control Assembly (Sheet 2 of 3)	7-34
Scope Power and Control Assembly (Sheet 3 of 3)	7-35
10.7 MHz Gen/Rec Module	7-19



SIGNAL SOURCE			SIGNAL DESTINATION		RECEIVE MODE		GENERATE MODE		DUPLEX MODE	
COAX NO.	CONNECTOR NO.	MODULE	CONNECTOR NO.	MODULE	LEVEL	FREQ/SIGNAL	LEVEL	FREQ/SIGNAL	LEVEL	FREQ/SIGNAL
1	J4202	LOW LOOP	J2203	IF BLOCK	+5 TO +12 dBm	77.3-79.3 MHz	+5 TO +12 dBm	77.3-79.3 MHz	+5 TO +12 dBm	77.3-79.3 MHz
2	J4203	LOW LOOP	J403	ANALYZER RF	-20 TO -40 dBm	77.3-79.3 MHz	-20 TO -40 dBm	77.3-79.3 MHz	-20 TO -40 dBm	77.3-79.3 MHz
3	J602	HI/LOW FILTER	J4101	HIGH LOOP	-28 dBm TO -34 dBm	90-1088 MHz	-28 dBm TO -34 dBm	90-1088 MHz	-28 dBm TO -34 dBm	90-1088 MHz
4	E2807	FREQ STANDARD	J4001	HIGH LOOP	4 V P-P (±.5 V)	500 kHz	4 V P-P (±.5 V)	500 kHz	4 V P-P (±.5 V)	500 kHz
5	J4103	HIGH LOOP	J1201	DUPLEX	-20 TO -30 dBm	90-1088 MHz	-20 TO -30 dBm	90-1088 MHz	-20 TO -30 dBm	90-1088 MHz
6	J4003	HIGH LOOP	J1906	DUAL VCO (1ST LO)	D.C.	0-35 VDC	D.C.	0-35 VDC	0-35 VDC	DC
7	J4002	HIGH LOOP	J1903	DUAL VCO (2ND LO)	D.C.	0 VDC	D.C.	0 VDC	0 VDC	DC
8	J1203	DUPLEX	J3513	DUPLEX CONNECTOR					-60 dBm	OFFSET GEN FREQ
9	J1204	DUPLEX	J5105	OUTPUT AMPLIFIER					-30 dBm	OFFSET GEN FREQ
10	J4303	10,7 MHz GEN/REC	J4401	DIGITAL	120 mV P-P (±10 mV)	10,7 MHz	120 mV P-P (±10 mV)	10,7 MHz	120 mV P-P (±10 mV)	10,7 MHz
11	J4304	10,7 MHz GEN/REC	J4502	DIGITAL	2,2 V P-P (±.2 mV)	21,4 MHz	2,2 V P-P (±.2 V)	21,4 MHz	2,2 V P-P (±.2 V)	21,4 MHz
12	E2806	FREQ STANDARD	J4503	DIGITAL	4,0 V P-P (±.5 V)	1 MHz	4,0 V P-P (±.5 V)	1 MHZ	4,0 V P-P (±.5 V)	1 MHz
13	J2202	IF BLOCK	J4302	10,7 MHz GEN/REC	INPUT ±2 dBm	10,7 MHz	-15 TO -20 dBm	10,7 MHz	INPUT ±2 dBm	10,7 MHz
14	J405	ANALYZER RF	J2208	IF BLOCK	INPUT	83-95 MHz	-28 dBm TO -32 dBm	88-90 MHz	INPUT	83-95 MHz
15	E2809	FREQ STANDARD	J404	ANALYZER RF	1,5 V P-P (±.2 V)	1 MHz	1,5 V P-P (±.2 V)	1 MHz	1,5 V P-P (±.2 V)	1 MHz
16	J401	ANALYZER RF	J502	ANALYZER IF	0 TO 5 dBc	22,3 MHz	-45 TO -60 dBc	22,3 MHz	0 TO 5 dBc	22,3 MHz
17	J503	ANALYZER IF	J802	ANALYZER LOG AMP	30 dBc	1,2 MHz	30 dBc	1,2 MHz	30 dBc	1,2 MHz
18	J3512	ANT CONNECTOR	J2201	IF BLOCK	INPUT	RF			INPUT	RF
19	J2202	IF BLOCK	J1501	OUTPUT AMPLIFIER			-20 dBm (±5 dB)	RF		
20	J5103	OUTPUT AMPLIFIER	AT3501-J1	ATTENUATOR			W/FINE ATTN CCW 0 dBm (±1 dB)	RF		
21	AT3501-J2	ATTENUATOR	J5102	OUTPUT AMPLIFIER			20 dB ABOVE SELECTED LEVEL	RF		
22	J3514	T/R CONNECTOR	J5104	OUTPUT AMPLIFIER			-20 TO -127 dBm	RF	-80 dBm	RF
23	J2209	IF BLOCK	J406	ANALYZER RF	INPUT	83-95 MHz	-28 dBm TO -32 dBm	88-90 MHz	INPUT	83-95 MHz
24	J6402	LOW PASS FILTER	J601	HI/LOW FILTER	-25 dBm TO -30 dBm	90-1088 MHz	-25 dBm TO -30 dBm	90-1088 MHz	-25 dBm TO -3 dBm	90-1088 MHz
25	J1907	DUAL VCO	J6401	LOW PASS FILTER	-22 dBm TO -28 dBm	90-1088 MHz	-22 dBm TO -28 dBm	90-1088 MHz	-22 dBm TO -28 dBm	90-1088 MHz
26	J1905	DUAL VCO	J9301	MIXER NULL	+5 TO +12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz
27	J1902	DUAL VCO	J2207	IF BLOCK	+5 to +12 dBm	1210 MHz	+5 TO +12 dBm	1210 MHz	+5 TO +12 dBm	1210 MHz
28	E2805	FREQ STANDARD	J4603	EXT REF CONNECTOR	130 mV P-P (±10 mV)	10 MHz	130 mV P-P (±10 mV)	10 MHz	130 mV P-P (±10 mV)	10 MHz
29	J3602	OPT OVEN OSC	E2808	FREQ STANDARD	1,5 V P-P (±.2 V)	10 MHz	1,5 V P-P (±.2 V)	10 MHz	1,5 V P-P (±.2 V)	10 MHz
30	J9302	MIXER NULL	J2205	IF BLOCK	+5 TO +12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz	+5 TO +12 dBm	1300-2298 MHz
31	J9303	MIXER NULL	J2210	IF BLOCK		1300-2298 MHz		1300-2298 MHz		

Figure 7-1 FM/AM-1200 System Block Diagram With Coax Numbers And Signal Flow Data

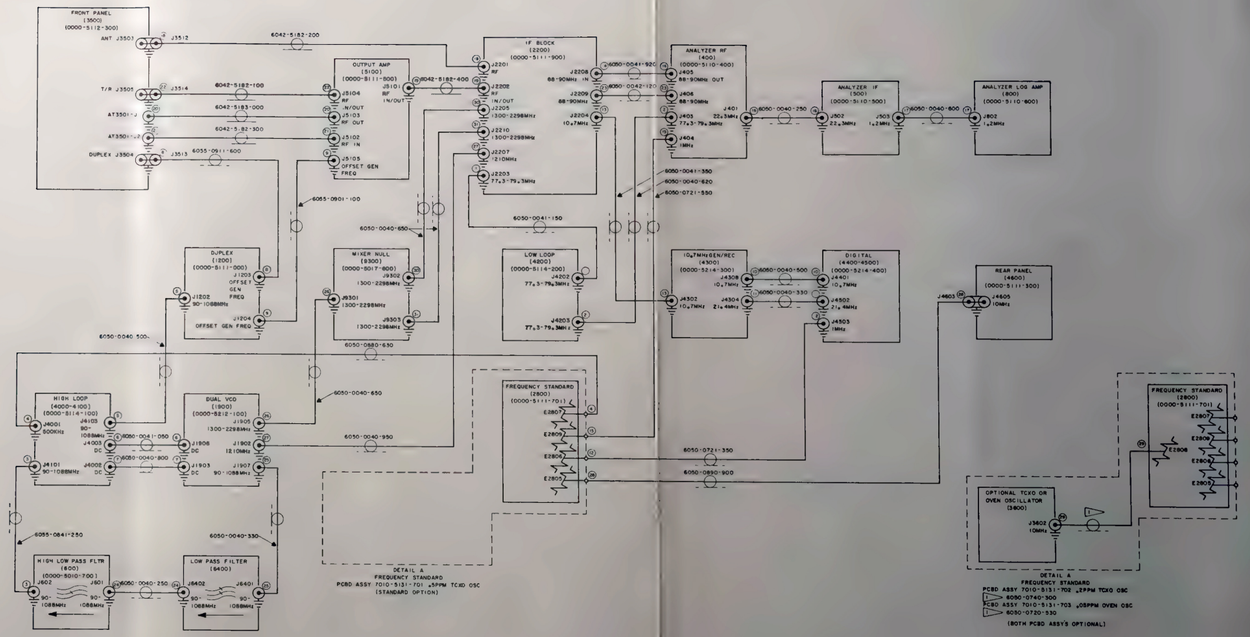


Figure 7-2 Coaxial Cable Interconnect Diagram (0000-5111-800-G)

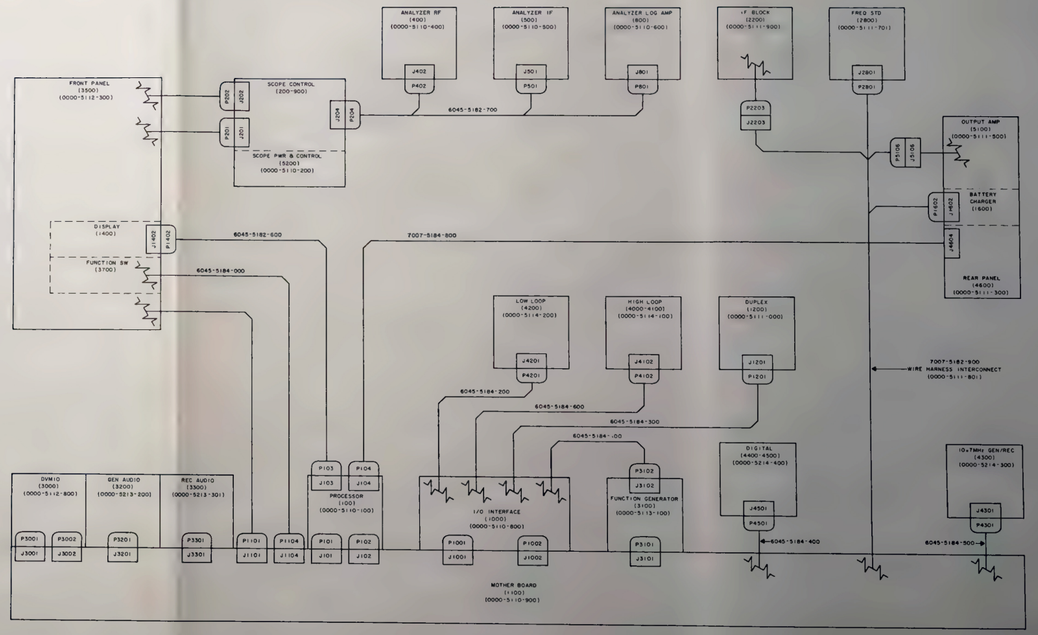


Figure 7-3 Ribbon Cable Interconnect Diagram (0000-5111-800-G)

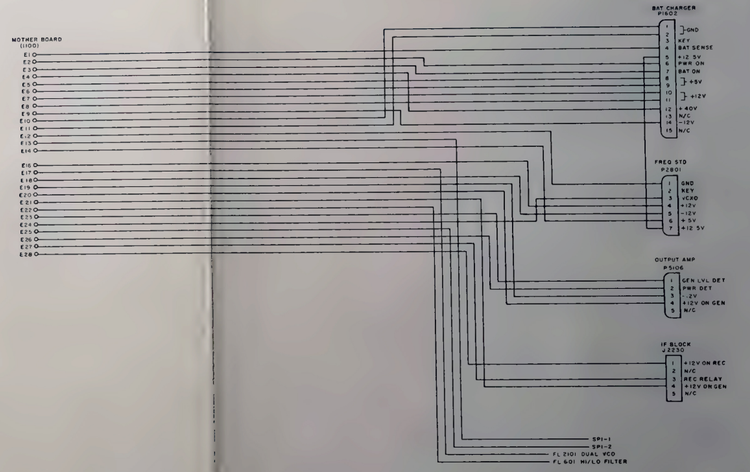
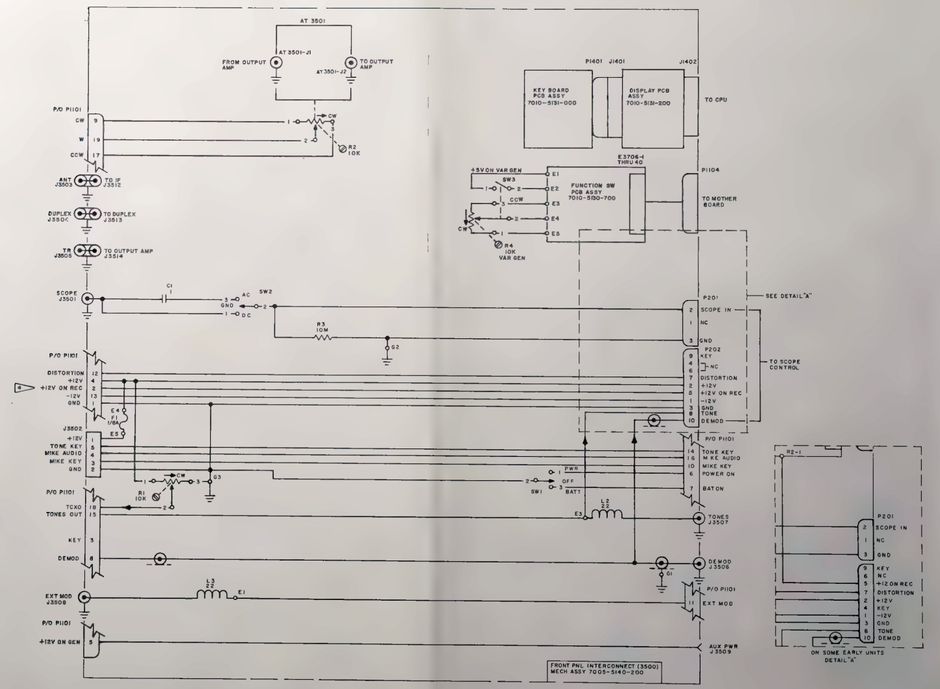


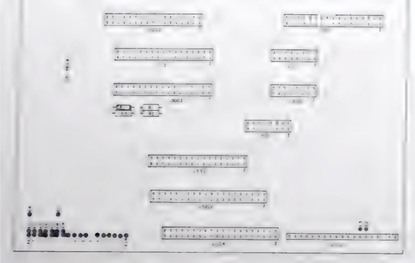
Figure 7-4 Main Wire Harness Diagram
(0000-5111-801)



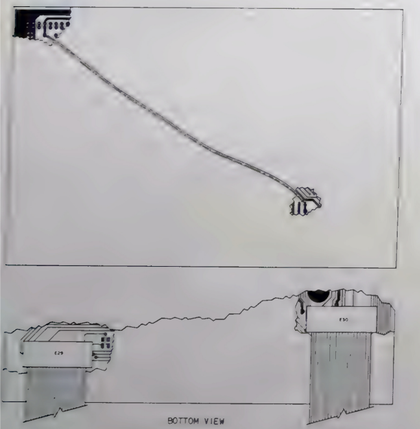
NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES 3500 (E.G., R1 IS R3501).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. P1101 - PIN 2 ON SOME EARLY UNIT WAS NC.
5. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

Figure 7-5 Front Panel Interconnect Diagram (0000-5112-300-H)

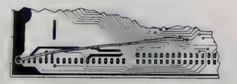


TOP VIEW



BOTTOM VIEW

Motherboard PC Board (Rev E-3)



BOTTOM VIEW
REV D ONLY

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 1100 (E.G., R1 IS R1101).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

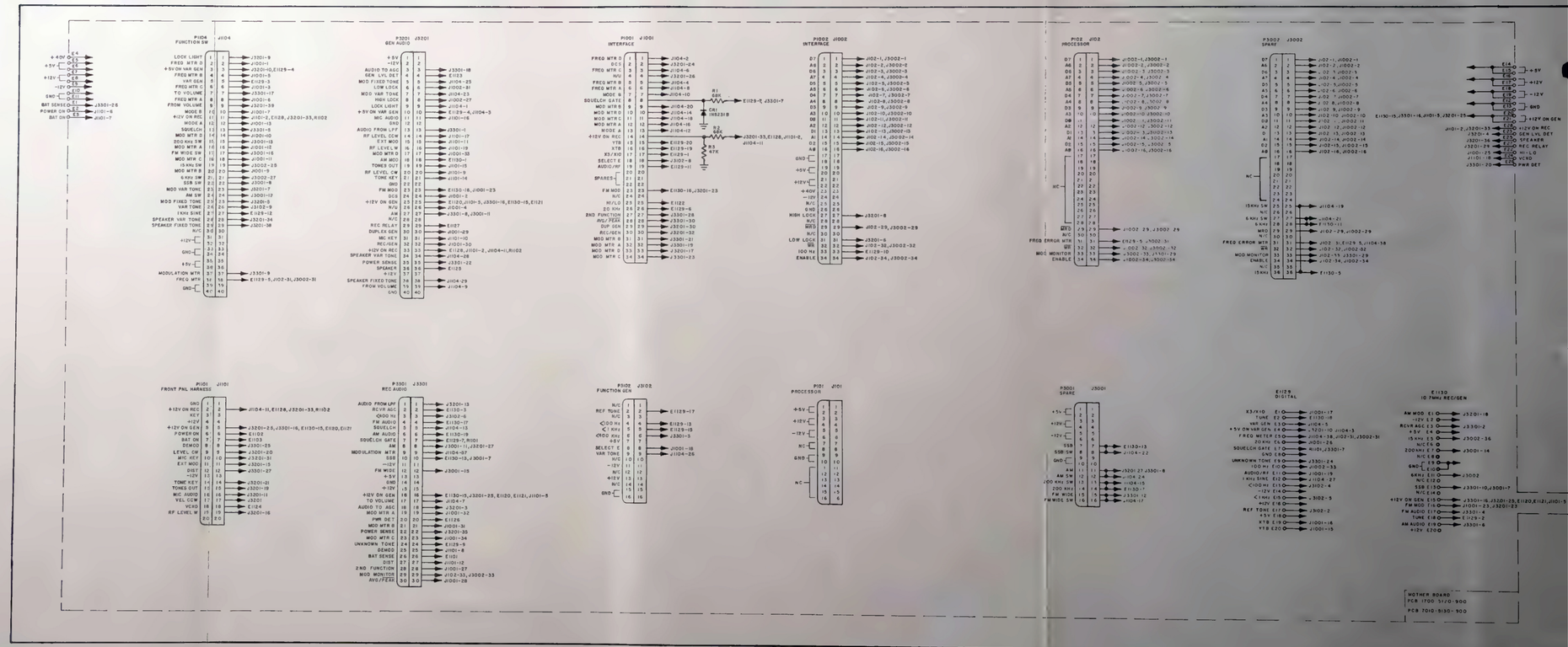
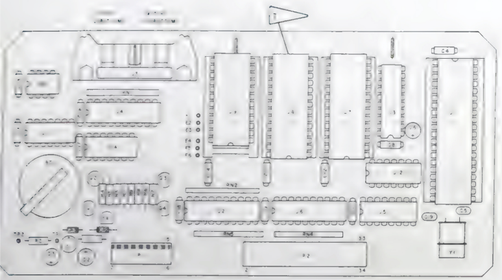
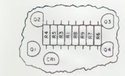
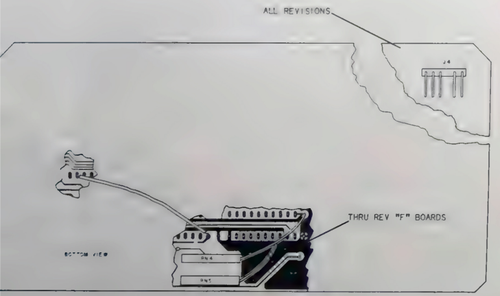


Figure 7-6 Motherboard PC Board Assembly (0000-5110-900-E3)





THRU REV "F" BOARDS



NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 100 (E.G., R1 IS R101).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED. PRECISION RESISTORS (1%) ARE DESIGNATED BY AN ASTERISK (*).
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. U9 IS A 24 PIN IC INSTALLED IN A 28 PIN SOCKET. THE PIN NUMBERS INDICATED ARE RELATIVE TO THE SOCKET AND NOT THE IC. THEREFORE, PIN 3 IS PIN 1 OF THE IC.
5. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.
7. U8 REQUIRED FOR -01 ASSY OPTION ONLY.

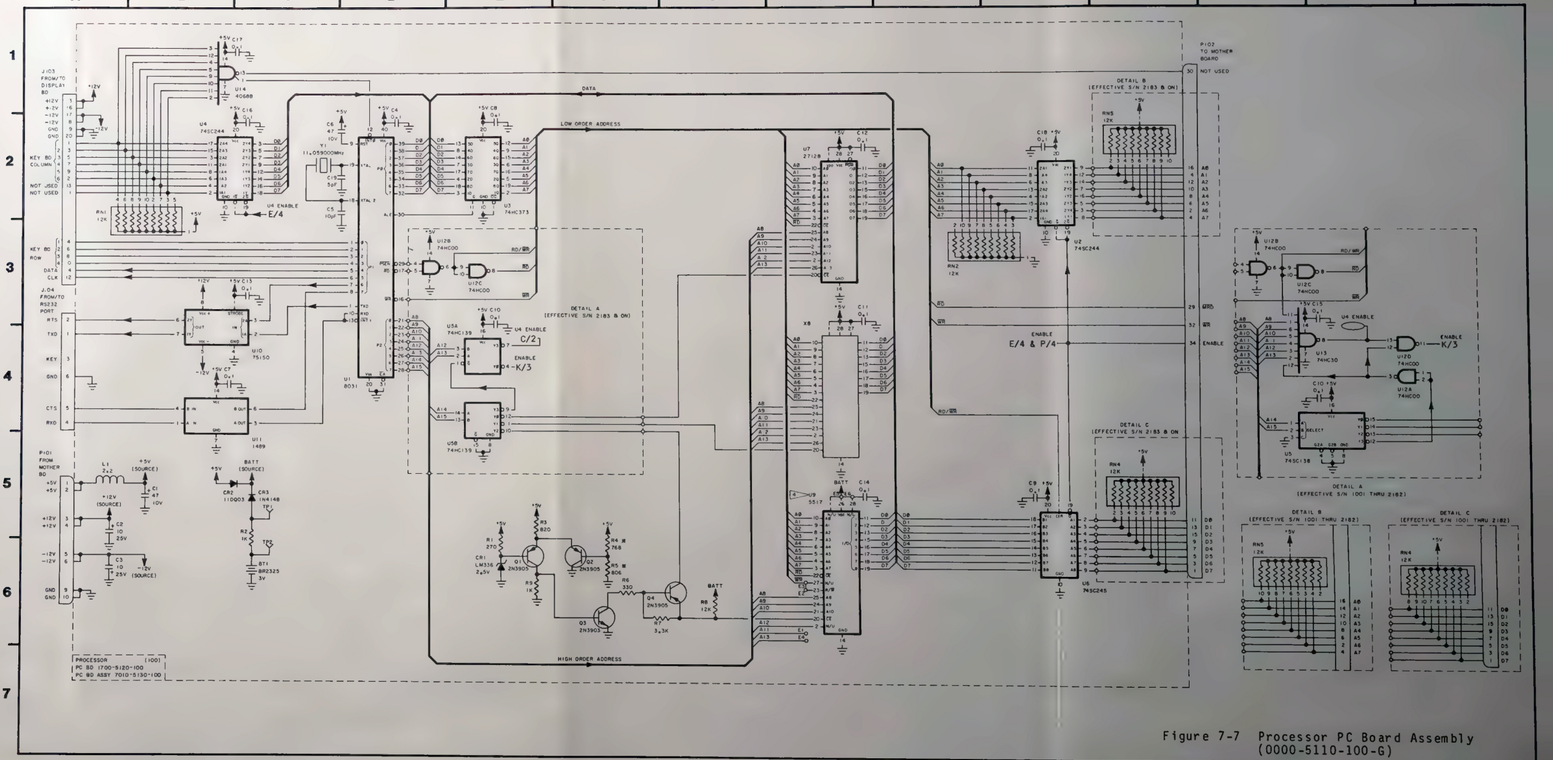
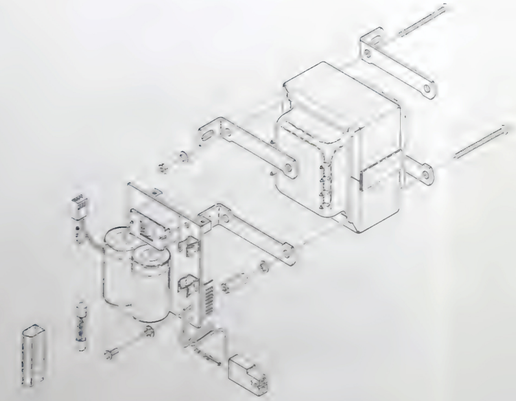
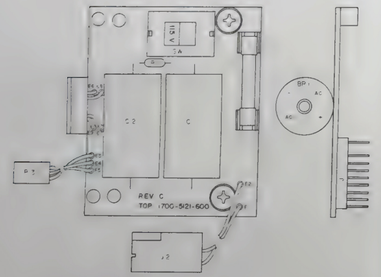
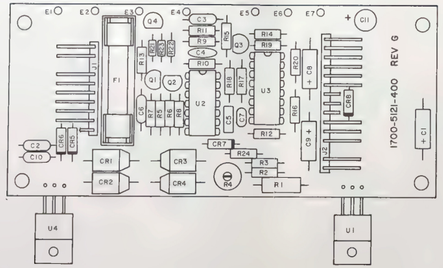


Figure 7-7 Processor PC Board Assembly (0000-5110-100-G)

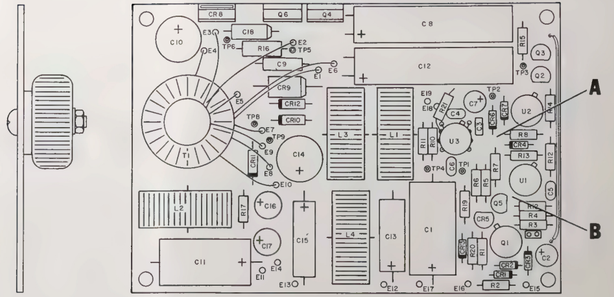


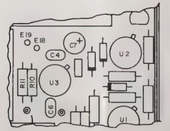


Line Supply PC Board Assy (Rev C-5)



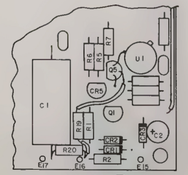
Battery Charger PC Board (Rev G-6)





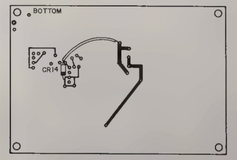
DETAIL A

EFF SN1468 THRU 1746



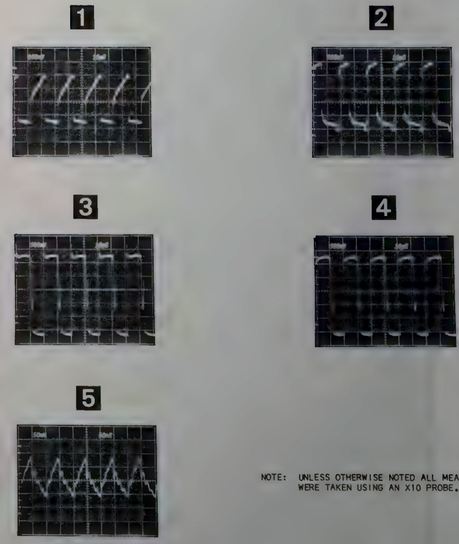
DETAIL B

EFF SN1001 THRU 1467



EFF SN1747 AND ON

Inverter Supply PC Board (Rev F-3)



NOTE: UNLESS OTHERWISE NOTED ALL MEASUREMENTS WERE TAKEN USING AN X10 PROBE.

Figure 7-8 Power Supply Module (Sheet 1 of 2)
(0000-5111-300-F2)
(0000-5111-400-G1)
(0000-5111-600-C2)

STANDARDS:
(UNLESS OTHERWISE NOTED)

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. 1500 (INVERTER SUPPLY PC BOARD).
   B. 1600 (BATTERY CHARGER PC BOARD).
   C. 1700 (LINE SUPPLY PC BOARD).
   D. 3900 (POWER SUPPLY MECH ASSY).
   E. 4600 (REAR PANEL MECH ASSY).
   F. (E,G, R1 IS R1501, ETC.)

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE. PRECISION RESISTORS (1%) ARE DESIGNATED BY AN ASTERISK (*).

3. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS.

4. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS.

NOTES: (INVERTER SUPPLY PC BOARD)

1. NOT USED.

2. NOT USED.

3. L1 THRU L4 ARE 30 TURNS OF 18 GA WIRE.

4. SN1001 THRU SN1408, Q1506 NOT USED.

5. SN1001 THRU SN1408, CR1513 NOT USED, R20 IS 47K, 1/4 W, 5% TOLERANCE.

6. SN1001 THRU SN1377, JTB1501 NOT USED.

7. SN1001 THRU SN1746, CR1514 AND R1521 NOT USED, R11 IS 4.75 K, 1/4 W, 5% TOLERANCE.

NOTES: (BATTERY CHARGER PC BOARD)

1. NOT USED.

2. NOT USED.

3. SN1001 THRU SN1045, CR1605 AND CR1606 ARE IN 4002 TYPE DIODES AND R1624 NOT USED.

4. SN1001 THRU SN1101, C1611 NOT USED.

5. DETAIL A EFFECTIVE WITH OVEN OSCILLATOR (.05 PPM) OPTION ONLY.

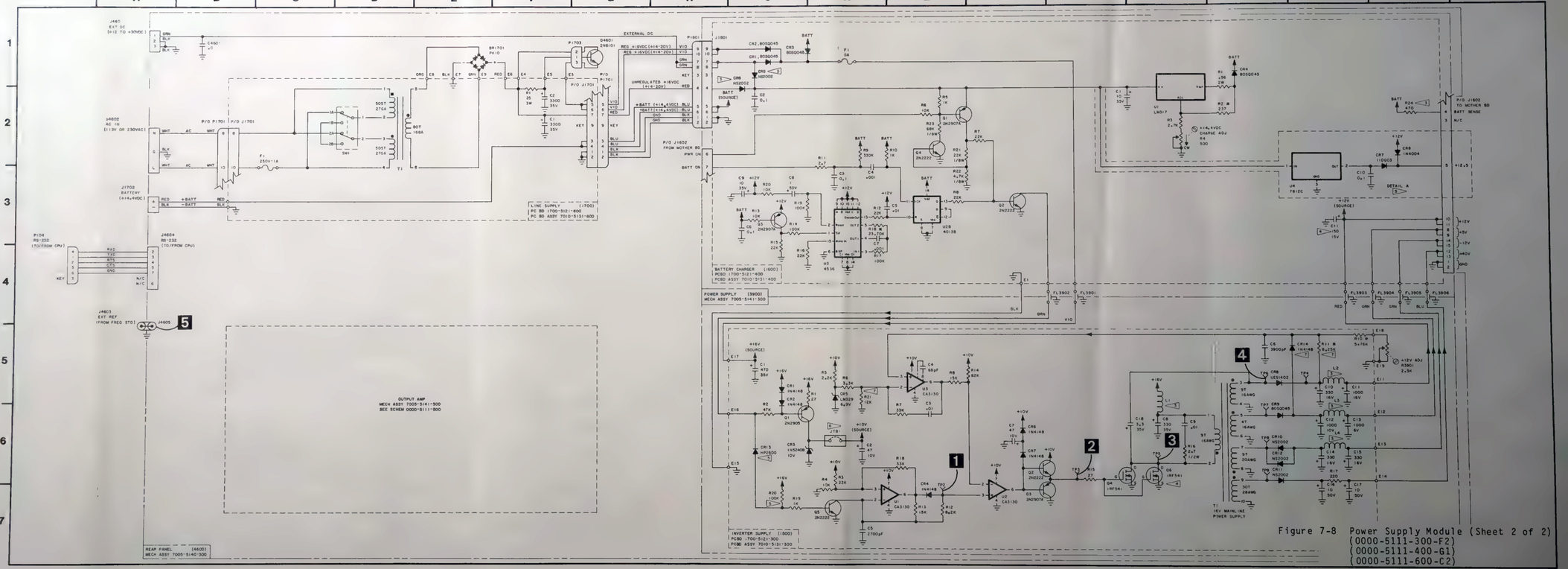
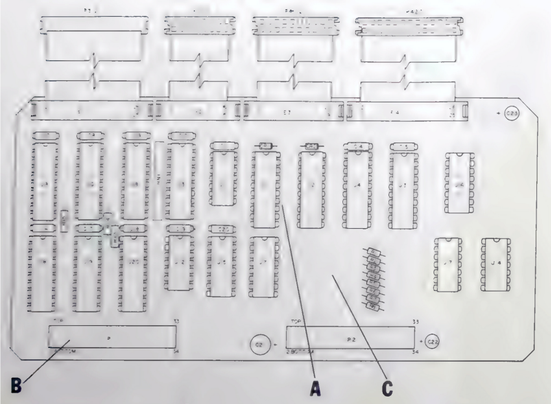


Figure 7-8 Power Supply Module (Sheet 2 of 2)
(0000-5111-300-F2)
(0000-5111-400-G1)
(0000-5111-600-C2)



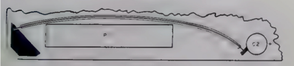
DETAIL **A**



EFF SN1001 THRU 1195

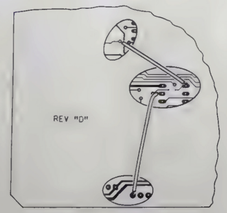


EFF SN1196 THRU REV "E"



DETAIL **B**

REV D ONLY

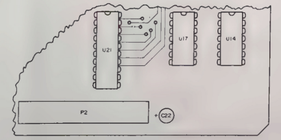


BOTTOM VIEW

Interface PC Board (Rev J-1)

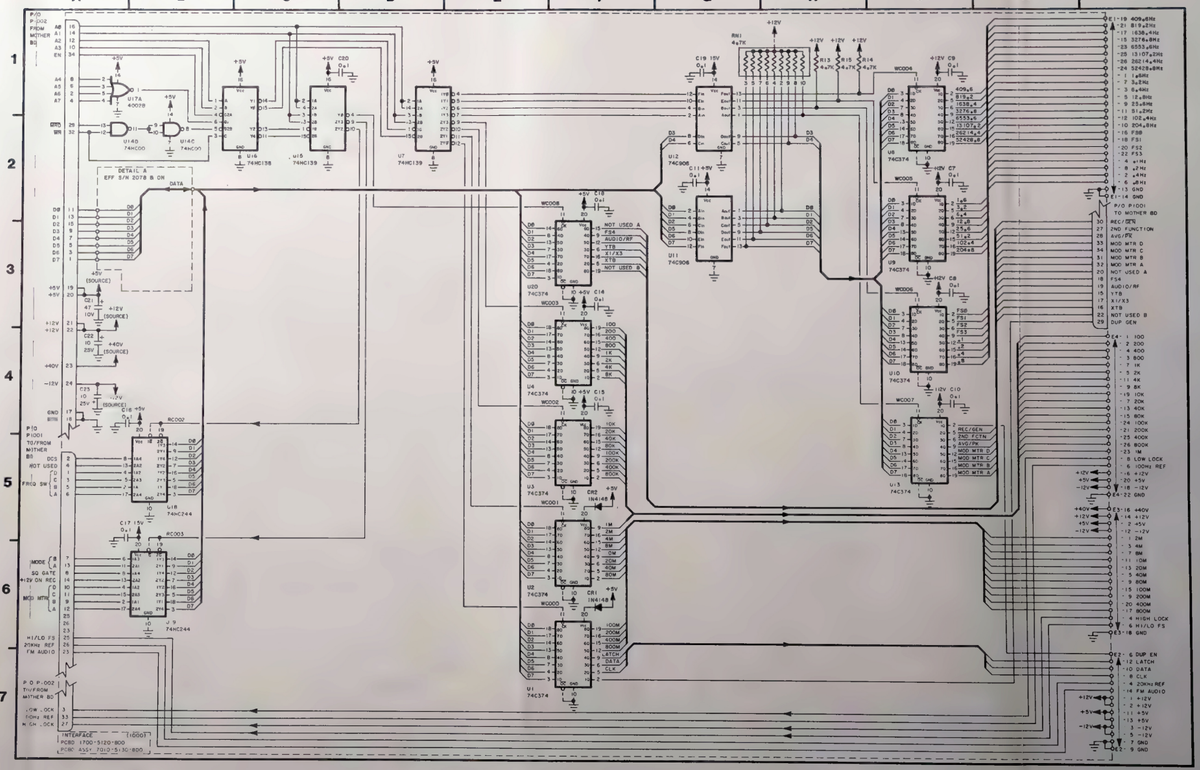
NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 1000 (E.G., R1 IS R1001).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. RESISTORS R1 THRU R8 ARE 100Ω, 1/8 W, 5% TOLERANCE.
5. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.



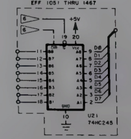
DETAIL **C**

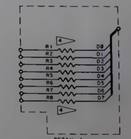
EFF SN1051 THRU 1467



MODULATION METER CONTROL (P10011)									
MOD METER CONTROL POSITION		INPUT				OUTPUT			
		MOD MTR A PIN 12	MOD MTR B PIN 9	MOD MTR C PIN 11	MOD MTR D PIN 10	MOD MTR A PIN 32	MOD MTR B PIN 31	MOD MTR C PIN 34	MOD MTR D PIN 33	AVG/PK PIN 28	2ND FUNC PIN 27
WP	150	0	0	0	0	0	0	0	0	0	0
	15	1	0	0	0	1	0	1	0	0	0
WA	150	0	1	0	0	0	1	0	1	0	0
	15	1	1	0	0	1	0	1	0	0	0
X1M/SX10	2	0	0	1	0	0	0	1	0	0	0
	6	1	0	1	0	1	0	1	0	0	0
	20	0	1	1	0	0	1	0	1	0	0
	60	1	1	1	0	1	0	0	0	0	1
BATT		0	0	0	1	0	0	0	0	0	0
SIG		1	0	0	1	1	0	0	0	0	0
DIST		0	1	0	1	0	1	0	1	0	0
SINAD		1	1	0	1	1	1	1	1	1	0
		1 = +5 VDC			0 = 0 VDC	1 = +12 VDC			0 = 0 VDC		

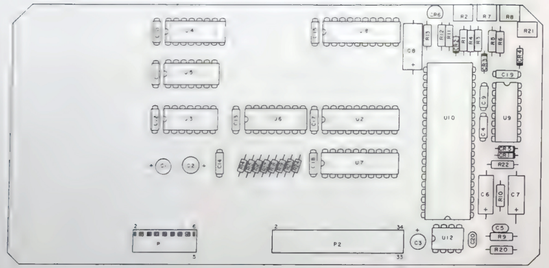
FREQ ERROR METER CONTROL (P10011)									
FREQ ERROR METER POSITION		INPUT				OUTPUT			
		FREQ SW A PIN 6	FREQ SW B PIN 5	FREQ SW C PIN 5	FREQ SW D PIN 1	XTB PIN 16	YTB PIN 15	X1/X3 PIN 17	AUDIO/INF PIN 19
RF	10	0	0	0	0	0	0	0	0
	100	0	0	0	1	0	0	1	0
	300	0	1	0	0	1	0	0	0
	1K	1	1	0	0	1	0	1	0
	3K	0	0	1	0	0	1	0	0
	10K	1	0	1	0	1	1	0	0
AUDIO	3	0	1	1	0	1	0	0	1
	30	1	0	1	0	0	1	0	1
	300	0	0	0	1	1	1	0	1
		1 = +5 VDC		0 = 0 VDC		1 = +5 VDC		0 = 0 VDC	



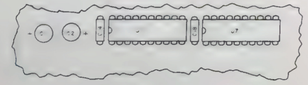


MODE CONTROL SWITCH				
MODE CONTROL POSITION	P1001 INPUT		P1001 OUTPUT	E1002-6 OUTPUT
	MODE A PIN 13	MODE B PIN 7	REC/GEN PIN 30	DUP GEN PIN 29	DUP ENABLE
GEN	0	0	0	0	1
REC	1	0	1	0	1
DUP	0	1	1	1	0
DUP/GEN	1	0	0	1*	1
	1 = +5VDC		0 = 0VDC	1 = 12VDC * = +5VDC	

Figure 7-9 Interface PC Board Assembly (0000-5110-800-J)



DVM I/O PC Board (Rev B-5)



EFF SN1001 THRU 1377



EFF SN1378 AND ON

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 3000 (E.G., R1 IS R3001).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

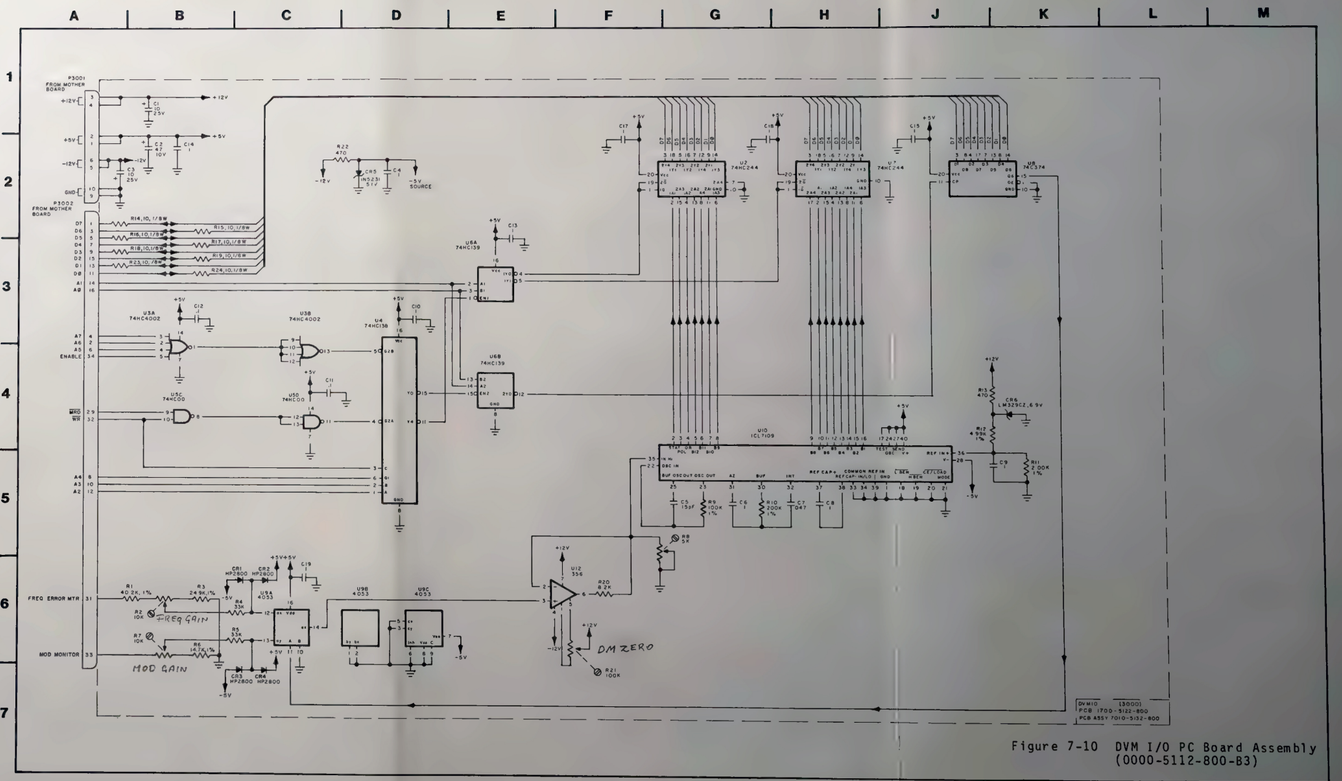
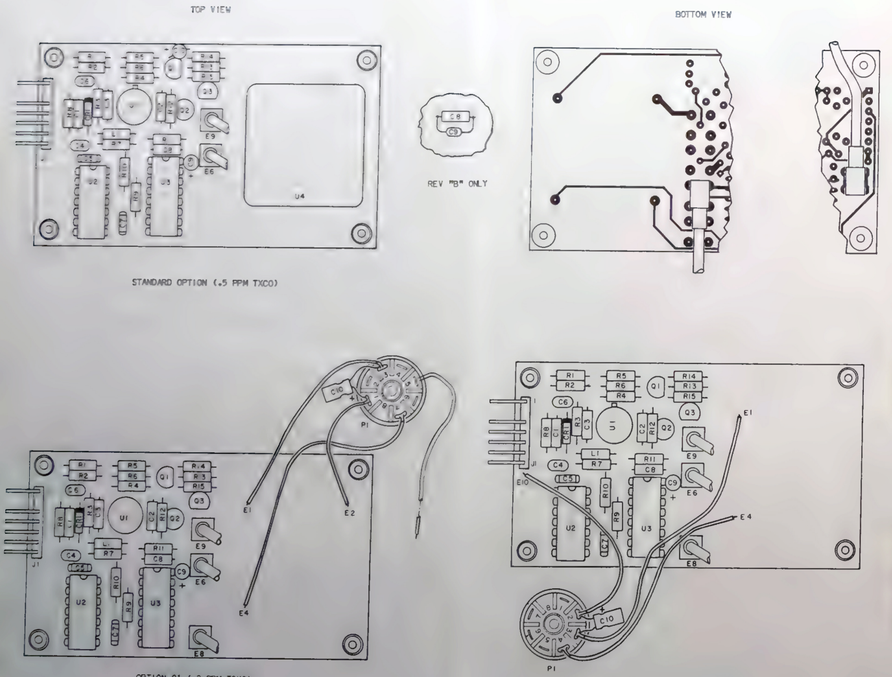


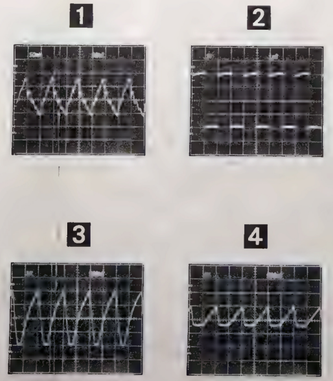
Figure 7-10 DVM I/O PC Board Assembly (0000-5112-800-B3)



Frequency Standard PC Board (Rev D-1)

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 2800 AND 3600 (E.G., R1 IS R2801, ETC.).
2. ONLY ONE (1) OSCILLATOR IS INSTALLED PER ASS'Y.
   - A. INSTALLED W/.05 PPM OSC ONLY.
   - B. INSTALLED W/.2 PPM OSC ONLY.
   - C. INSTALLED W/.5 PPM OSC ONLY.
3. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
4. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
5. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.



NOTE: ALL MEASUREMENTS WERE TAKEN USING A BNC TEE CONNECTOR WITH AN X1 PROBE.

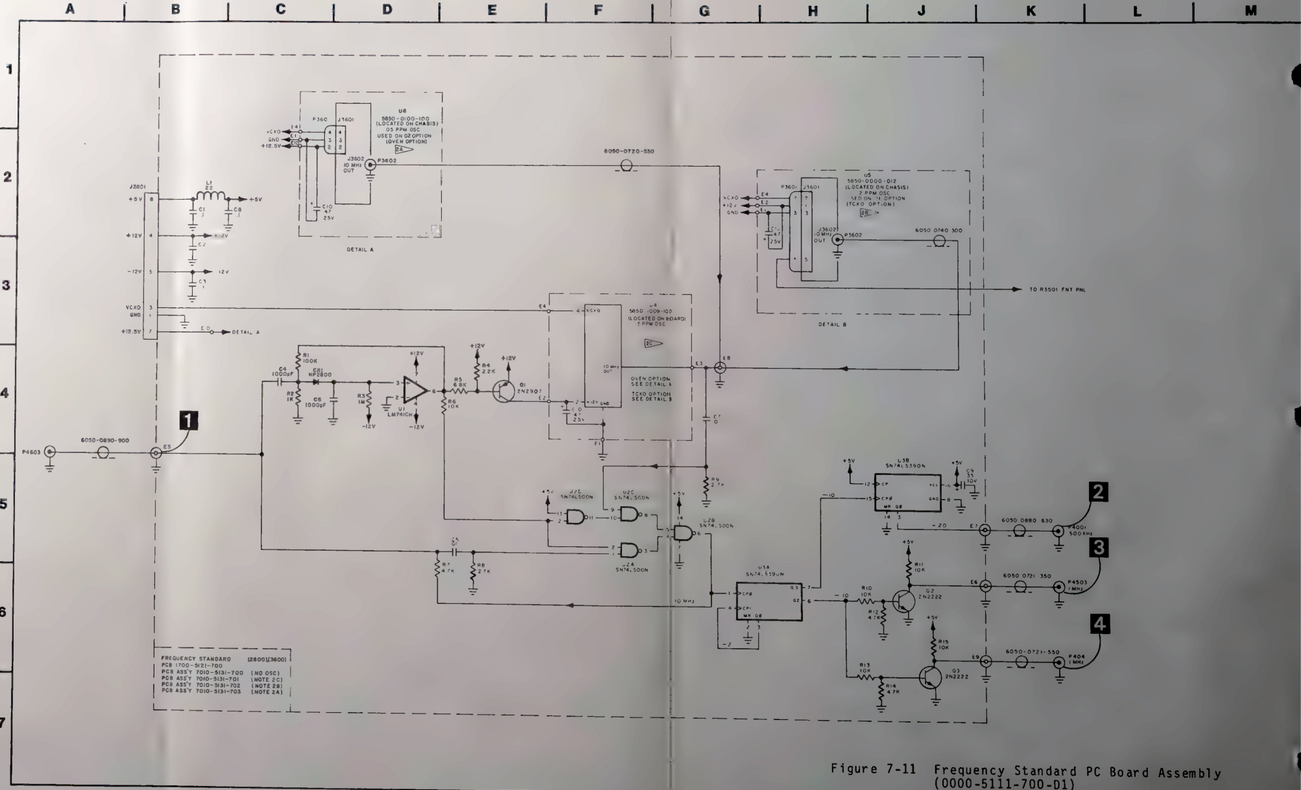
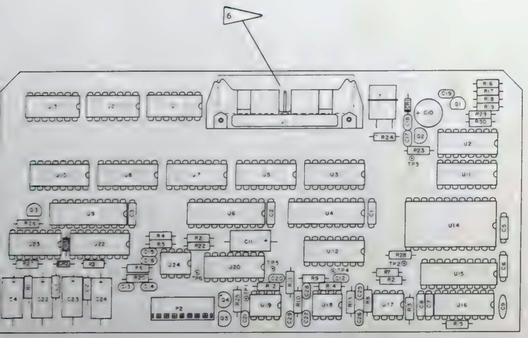


Figure 7-11 Frequency Standard PC Board Assembly (0000-5111-700-D1)



Function Generator PC Board (Rev B-7)

P3102 PIN #	IDENTIFIER	REMARKS
4	<100 Hz	HIGH (+12 VDC) WHEN SELECTED TONE IS LESS THAN 102.4 Hz
6	<400 Hz	HIGH (+12 VDC) WHEN SELECTED TONE IS LESS THAN 409.6 Hz
5	< 1 kHz	HIGH (+12 VDC) WHEN SELECTED TONE IS LESS THAN 819.2 Hz

FUNCTION SELECT CONTROL LINES					
FUNCTION	A	B	C	D	E
SINE	0	0	0	0	0
SQUARE	1	0	0	0	0
RAMP	0	1	0	0	0
TRIANGLE	1	1	0	0	0
DTMF	X	X	1	0	1
PULSE	0	0	0	0	0
DCS	0	0	0	1	1

X = SELECT LINES A & B ARE HI IN DTMF WHEN NO TONE IS GENERATED, BOTH GO LOW WHEN GENERATING A TONE.

FUNCTION SELECTED	FILTER USED
S.NEWAVE AND DCS	
<819.2 hz	1 kHz
819.2 THRU 13106.2 Hz	10 kHz
13106.2 Hz	60 kHz
SQUARE, RAMP, AND TRIANGLE	
<819.2 Hz	10 kHz
2819.2 Hz	60 kHz
DTMF	1 kHz

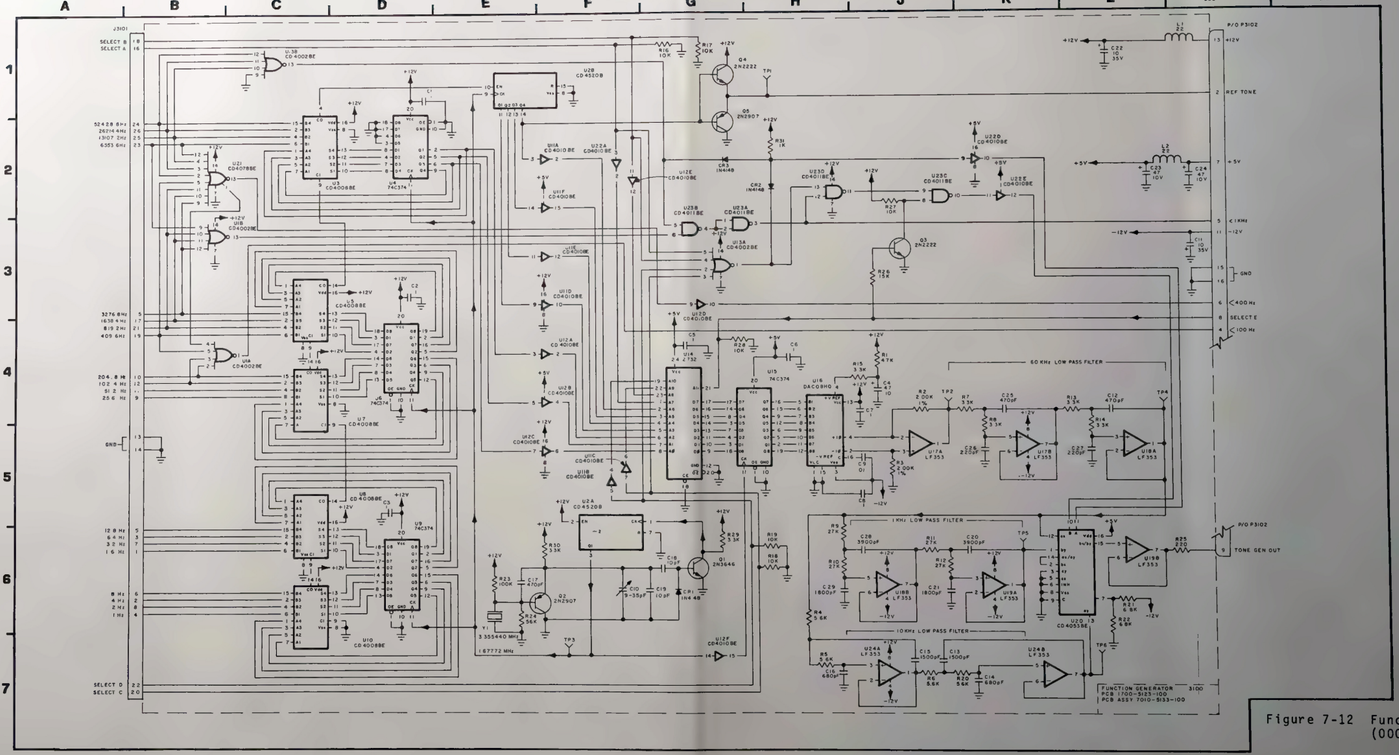
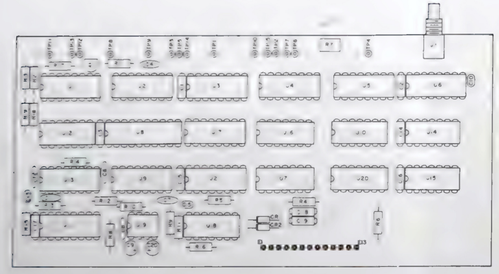


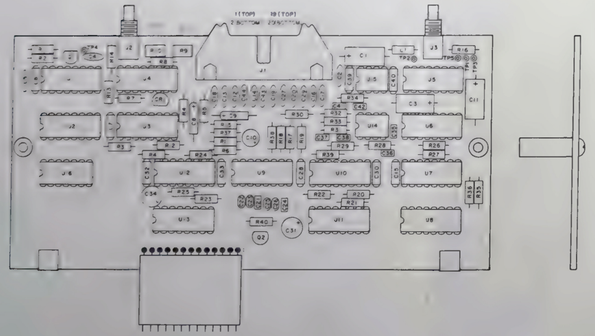
Figure 7-12 Function Generator PC Board Assembly (0000-5113-100-B5)

NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 3100. (E.G., R1 IS R3101).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.
6. APPLY TWO STRIPS OF MYLAR TAPE (1/4" WIDE X 1 3/4" LONG).



Digital Counter PC Board (Rev B)

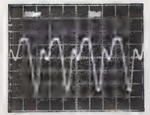


Digital Reference PC Board (Rev F-2)

FREQ ERROR SELECT CODING									
J4501	53702 FREQ ERROR METER RANGE POSITION								
		RF					AUDIO		
PIN #	IDENTIFIER	30	100	300	1K	3K	10K	3	30	300
1	X5/X10	0	1	0	1	0	1	0	0	0
11	AUDIO/RF	0	0	0	0	0	0	1	1	1
19	XTB	0	0	1	1	0	0	1	0	1
20	XTB	0	0	0	0	1	1	0	1	1
TIME BASE		10 Hz		100 Hz	1 kHz			300 Hz	1 kHz	10 kHz
J4501 PIN #2 (GEN TUNE) IS TYPICALLY +5.0 VDC										

TEST POINTS	RF SETTINGS					
	30	100	300	1K	3K	10K
TP4401	0	0	1	1	0	0
TP4402	1	1	1	1	1	1
TP4403	0	0	0	0	1	1
TP4404	1	1	1	1	0	0
TP4405	1	1	0	0	0	0
TP4406	1	1	0	0	1	1
TP4407	0	0	1	1	1	1

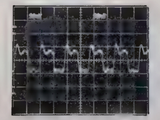
1



2



3



NOTE: ALL MEASUREMENTS WERE TAKEN USING A BNC TEE CONNECTOR WITH AN X1 PROBE.

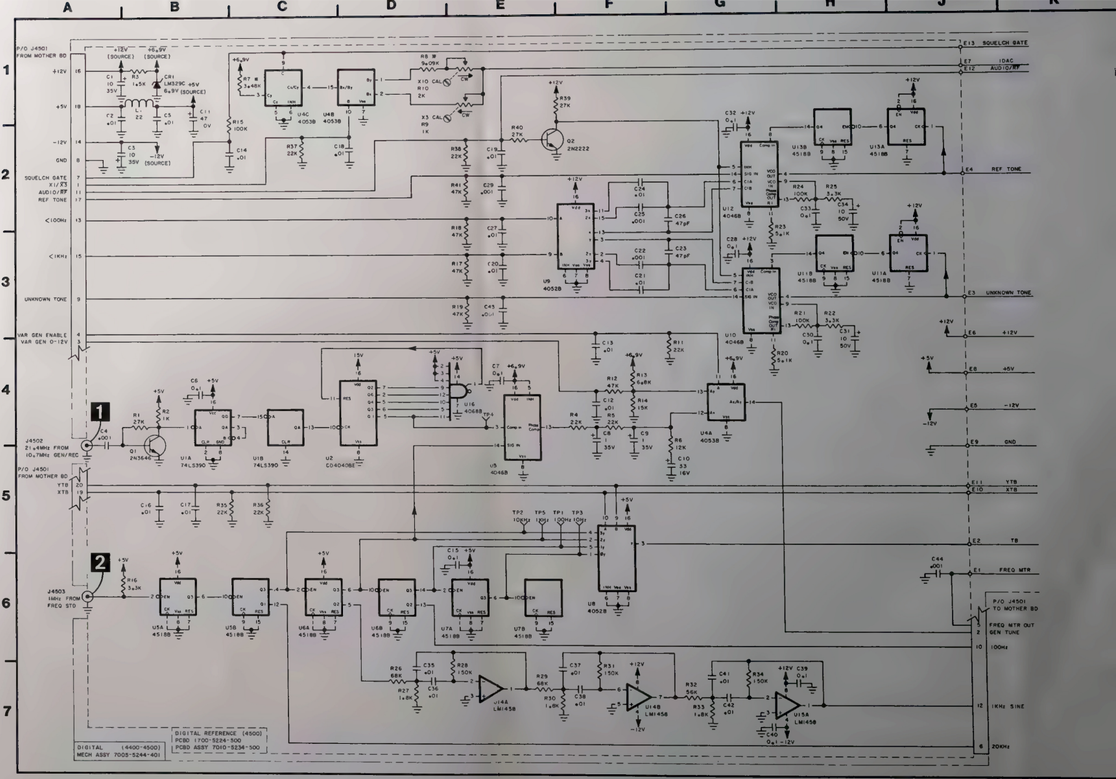
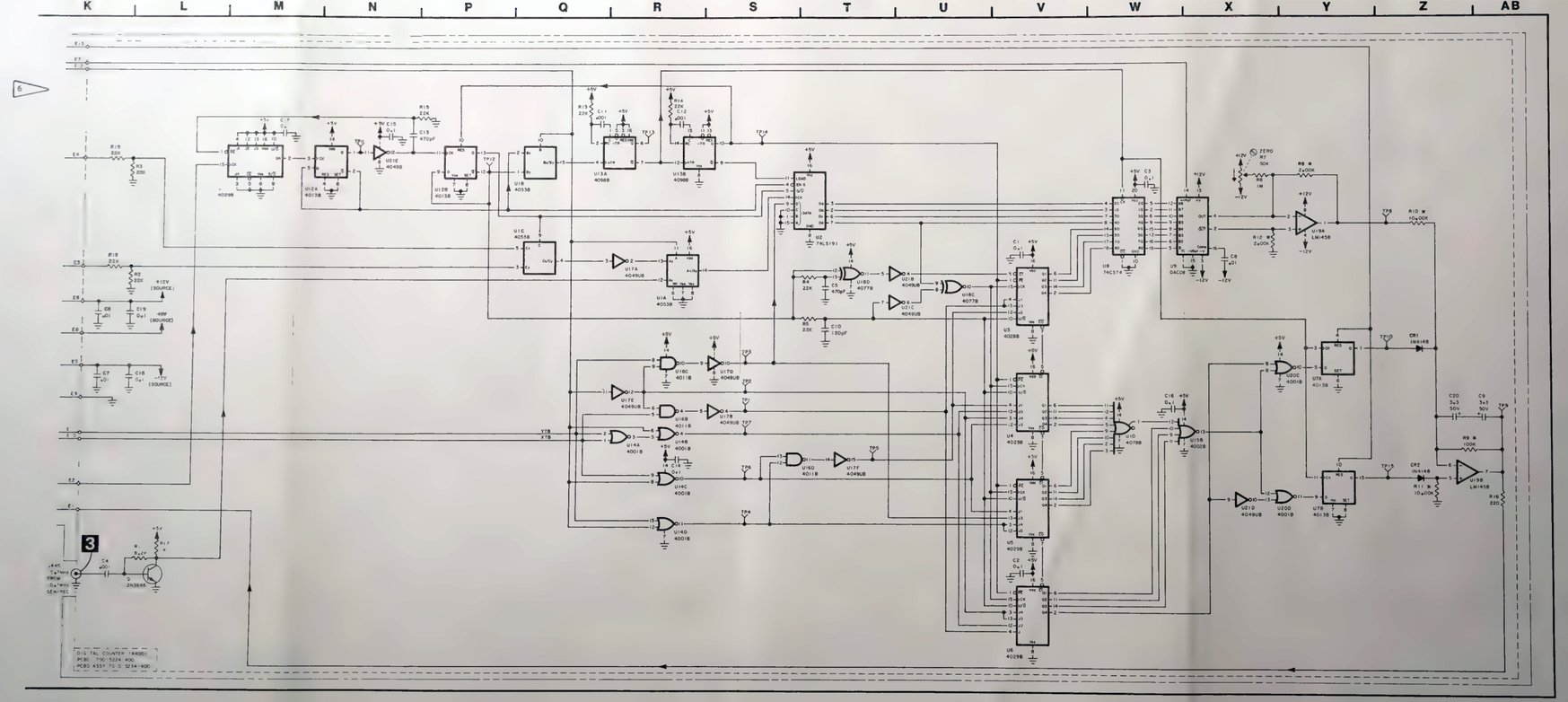


Figure 7-13 Digital Module (Sheet 1 of 2)
(0000-5214-400-C1)
(0000-5214-500-D)



NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. 4400 (DIGITAL COUNTER PC BOARD).
   B. 4500 (DIGITAL REFERENCE PC BOARD).
   C. (E.G., R1 IS R4401, ETC.).

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.

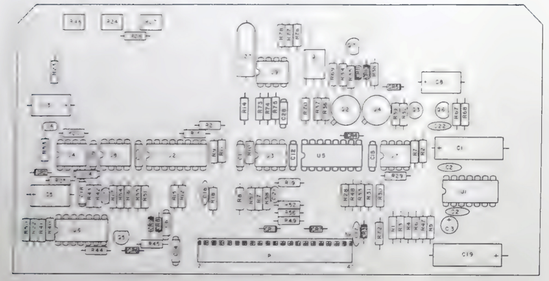
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

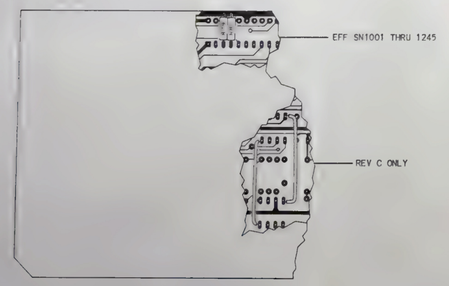
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

6. E POINTS ON DIGITAL ANALOG PC BOARD ARE JUMPERED TO E POINTS ON DIGITAL COUNTER PC BOARD (E.G., E1 ON ANALOG BD CORRESPONDS TO E1 ON DIGITAL BD).

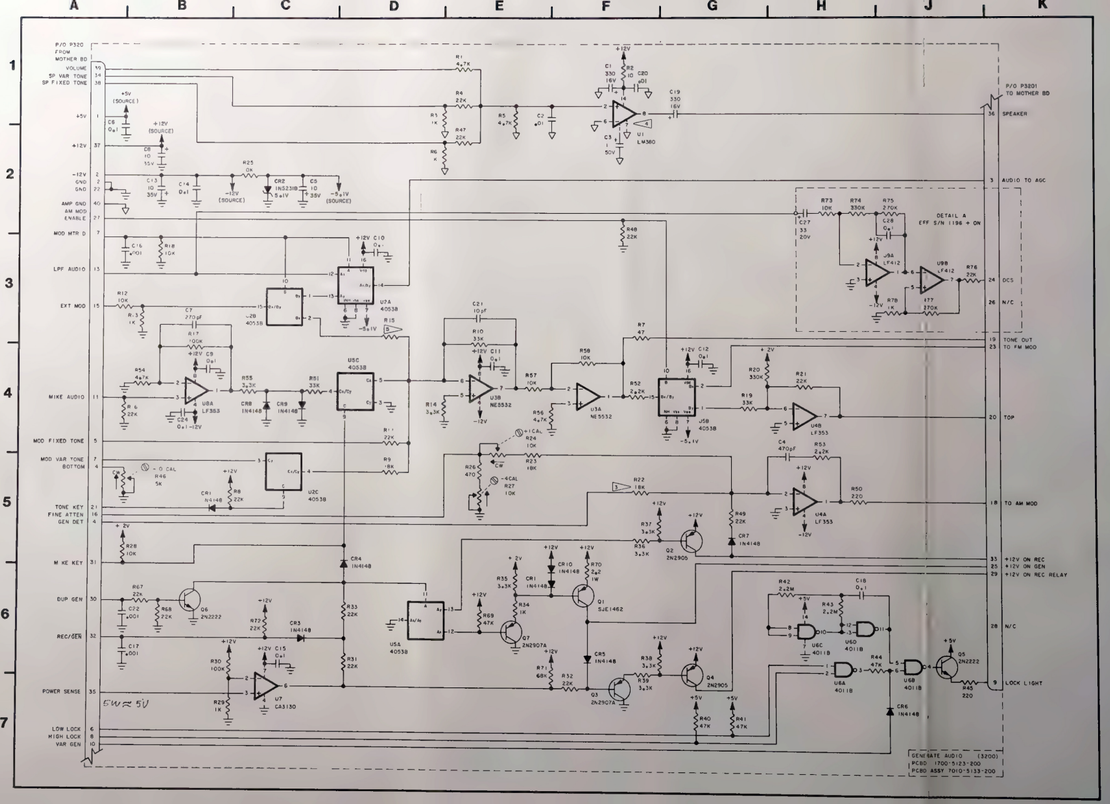
Figure 7-13 Digital Module (Sheet 2 of 2)
(0000-5214-400-C1)
(0000-5214-500-D)





Generate Audio PC Board (Rev P-1B)

P3201		REMARKS
PIN	IDENTIFIER	
4	GEN LVL DET	POSITIVE D.C. VOLTAGE PROPORTIONAL TO R.F. DETECTED IN THE OUTPUT AMP
6	LOW LOCK	+5 VDC WHEN LOW LOOP IS PHASE LOCKED
8	HIGH LOCK	+5 VDC WHEN HIGH LOOP IS PHASE LOCKED
17	MOD MTR D	+12 VDC WHEN MODULATION METER CONTROL IS IN DIST OR SINAD
21	TONE KEY	GROUND ON THIS LINE, WHEN IN GEN MODE, DISABLES FUNCTION GENERATOR OUTPUT
27	AM	+12 VDC WHEN MODULATION SELECT CONTROL IS IN AM NORM, AM NAR, AND SSB
31	MIKE KEY	GROUND WHEN MICROPHONE PTT SWITCH IS DEPRESSED
35	POWER SENSE	POSITIVE DC VOLTAGE PROPORTIONAL TO THE STRENGTH OF ANT RF RECEIVED AT THE T/R CONN



NOTES:

1. ALL REFERENCE DESIGNATORS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 3200 (E.G., R1 IS R3201).
2. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
3. SN1001 THRU SN1747, R22 IS A 15 K, 1/4 W, 5% TOLERANCE RESISTOR.
4. PINS 3, 4, 5, 10, 11 AND 12 ARE GROUNDED FOR HEAT DISSIPATION.
5. R15 IS SELECTED AT TEST (SAT), NOMINAL IS 5.6 K, RANGE IS 2.7 K TO 8.2 K.
6. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
7. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
8. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

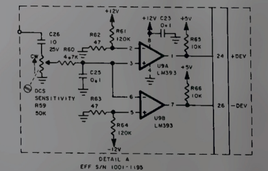
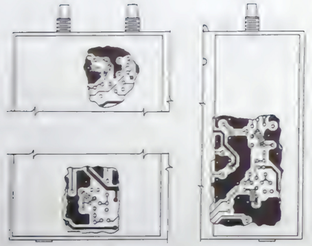


Figure 7-14 Generate Audio Module (0000-5113-200-D2)



BOTTOM VIEW

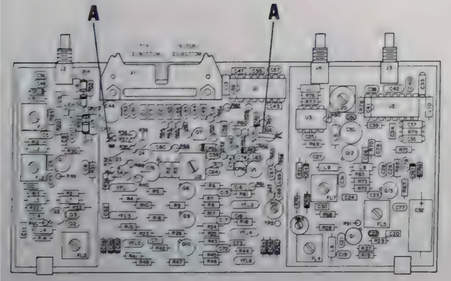
EFF SN1001 THRU 2182



EFF SN1001 THRU 2182

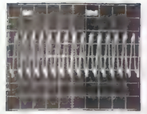


DETAIL A



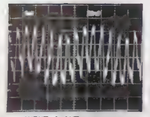
10.7 MHz Gen/Rec PC Board (Rev R)

1



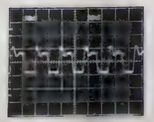
REC MODE
NO SIGNAL PRESENT

1

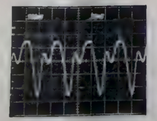


INPUT @ ANT.
(150.2 MHz @ -50 dB)

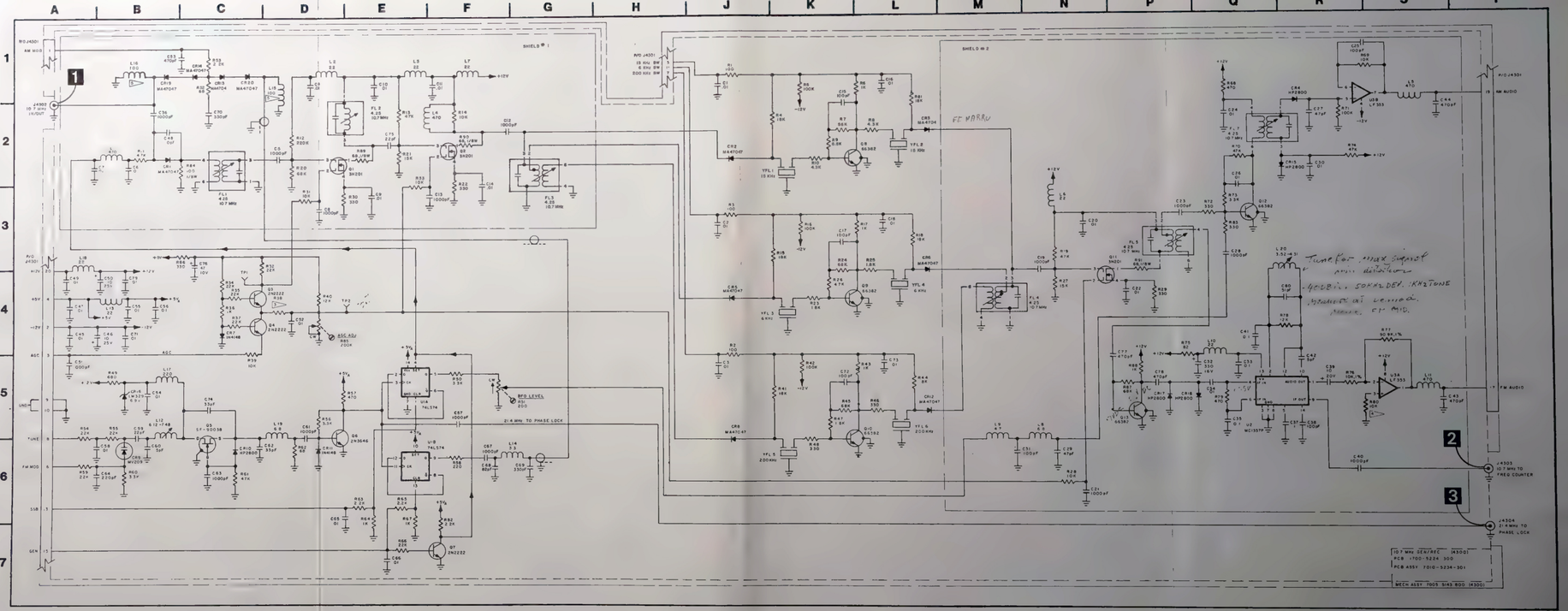
2



3



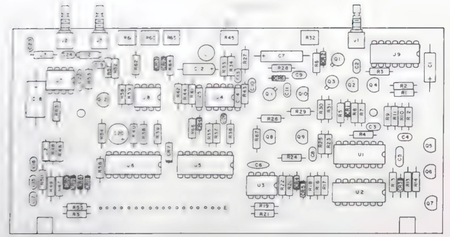
NOTE: ALL MEASUREMENTS WERE TAKEN USING AN X10 PROBE.



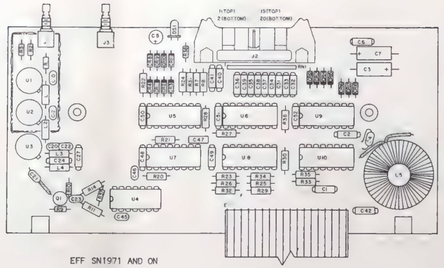
NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 4300 (E.G., R1 IS R4301).
2. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
3. R38 IS SELECTED AT TEST (SAT). NOMINAL IS 6.8 K, RANGE IS 4.7 K TO 15 K.
4. SN1001 THRU SN1055, R80 IS 150 K.
5. CR19 AND CR20 NOT USED IN SN1001 THRU SN2182.
6. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
7. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
8. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

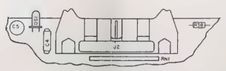
Figure 7-15 10.7 MHz Gen/Rec Module (0000-5113-800-J)



EFF SN2077 AND ON



EFF SN1971 AND ON



EFF SN1001 THRU 1970

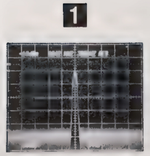


EFF SN1001 THRU 2076

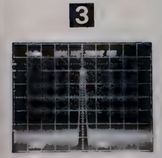
High Loop Analog PC Board (Rev C-1)

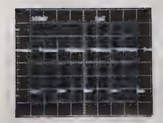


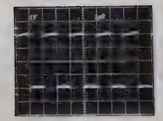
High Loop Divider PC Board (Rev E-2)



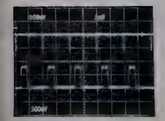




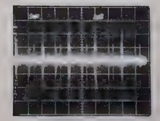




X1 PROBE



TOP TRACE Q11, PIN S
BOTTOM TRACE Q11, PIN G



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200 FREQUENCY SET ON 150.2 MHz USING AN X10 PROBE.

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:
   A. 4000 (HIGH LOOP ANALOG PC BOARD).
   B. 4100 (HIGH LOOP DIVIDER PC BOARD).
   C. (E.G., R1 IS R4001, ETC.).
2. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
3. R4137 IS SELECTED AT TEST (SAT). NOMINAL IS 33 OHMS. RANGE IS 22 OHMS TO 56 OHMS.
4. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
5. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

Figure 7-16 High Loop Module (Sheet 1 of 2) (0000-5114-100-C)

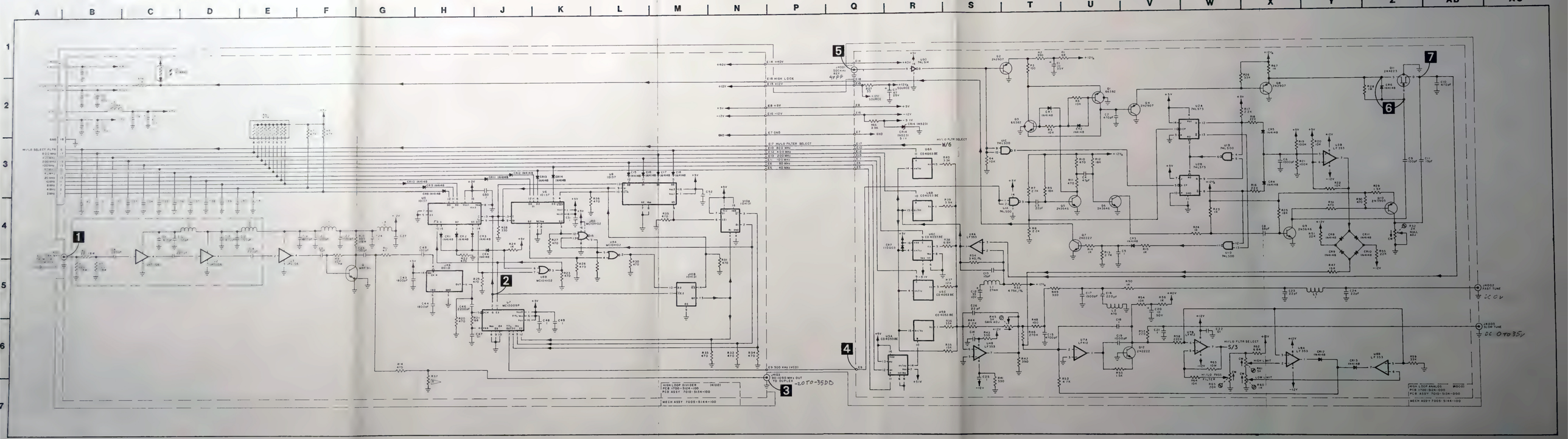
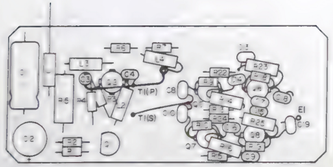
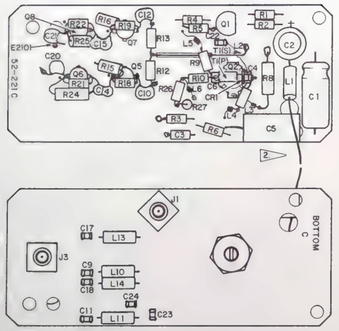


Figure 7-16 High Loop Module (Sheet 2 of 2)
(0000-5114-100-C)



1210 MHz VCO PC Board (Rev H)



1300-2300 MHz VCO PC Board (Rev R)



VCO Mixer Assembly (Rev C)

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. 1900 (VCO MIXER PC BOARD).
   B. 2000 (1210 MHz VCO PC BOARD).
   C. 2100 (1300-2298 MHz VCO PC BOARD)
   D. (E.G., R1 IS R1901, ETC.).

2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.

3. PRIMARY (T2001) IS FORMED BY LEAD OF C2004 PLACED 0.38 INCHES FROM SECONDARY. SECONDARY T2001 IS FORMED BY 22 GA WIRE 0.8 IN. LONG.

4. 10 TURNS, 38 GA WIRE 0.014 IN. DIA.

5. PRIMARY T2101 IS FORMED BY LEAD OF C2106 SOLDERED TO CR2101, LENGTH SELECTED AT TEST (SAT). SECONDARY T2101 IS 22 GA WIRE BENT TO WITHIN 0.4 IN. OF BOARD SURFACE THEN BACK TO WITHIN 0.2 IN. OF PRIMARY.

6. R2108 IS SELECTED AT TEST (SAT). NOMINAL IS 180Ω. RANGE IS 47Ω TO 220Ω.

7. TORRIOD 18 GA, 30 TURNS.

8. SN1001 THRU SN1651, C6 IS 1200 pF.

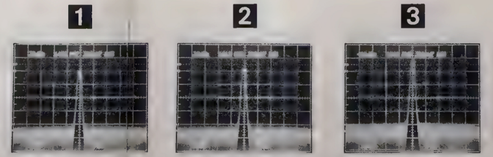
9. SN1001 THRU SN1045, C25 NOT USED.

10. SN1001 THRU SN2077, R6 IS 56Ω.

11. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

12. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.

13. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200 FREQUENCY SET ON 150.2 MHz.

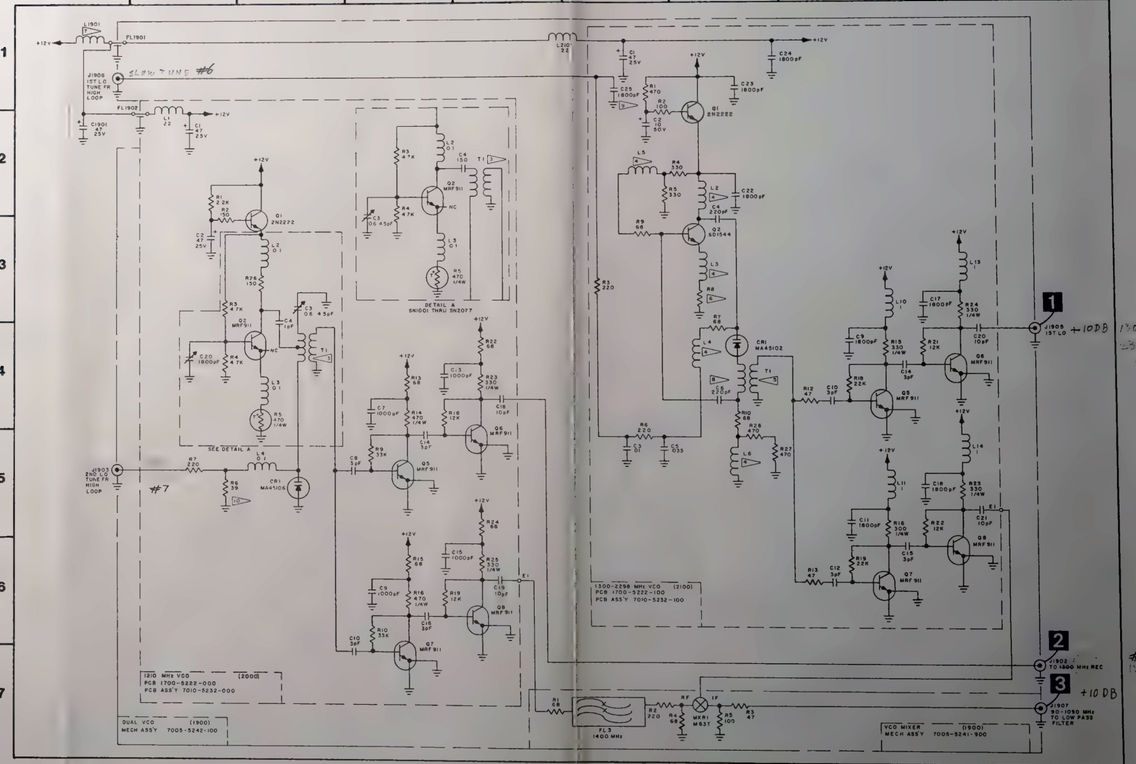
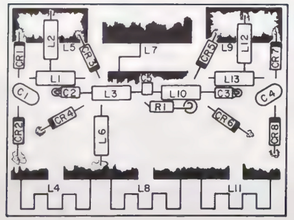
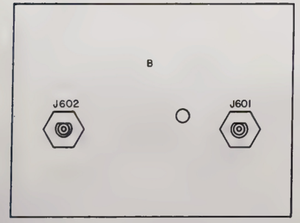


Figure 7-17 Dual VCO Module (0000-5212-100-L)

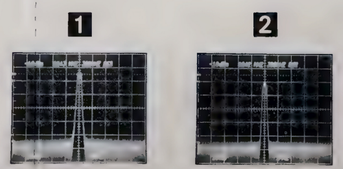




High/Low Pass Filter PC Board (Rev B-3)

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 600 AND 700 (E.G., C1 IS C701).
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.
6. ALL SHADED AREAS INDICATE MICRO-STRIPPING.
7. L4, L5, L7, L8, L9, AND L11 ARE PRINTED CIRCUIT COMPONENTS.



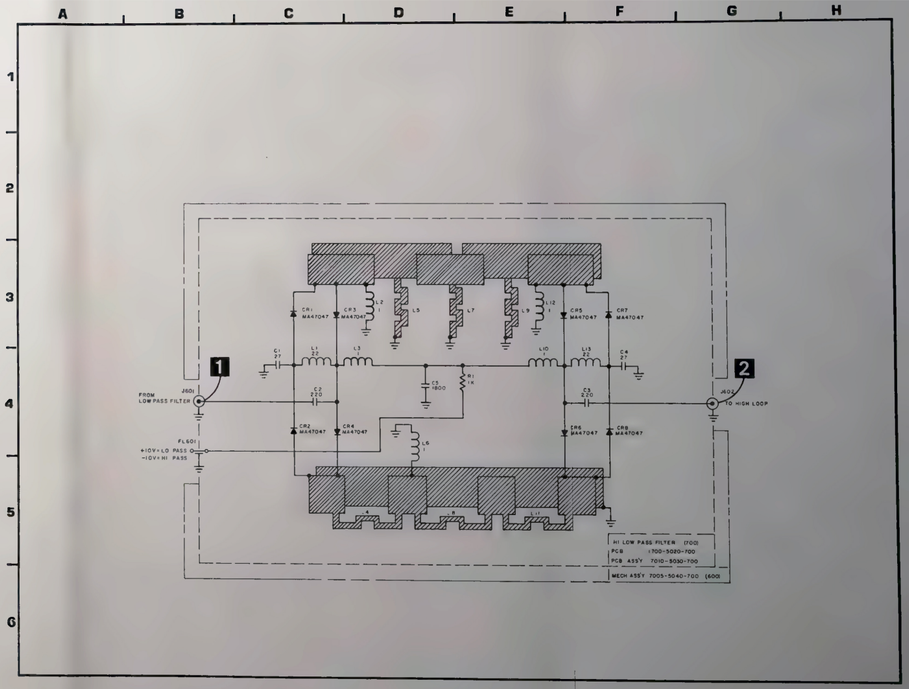
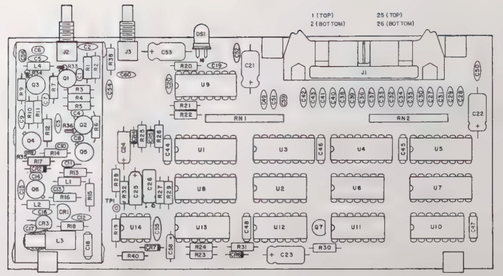
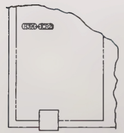


Figure 7-18 High/Low Pass Filter Assembly (0000-5010-700-B)





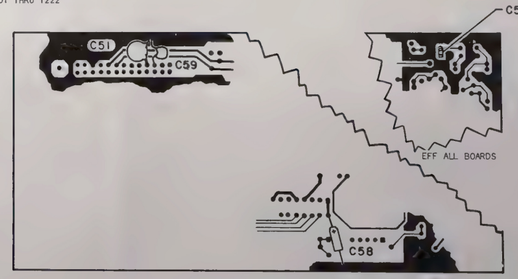
EFF SN1001 THRU 1222



EFF SN1001 THRU 2845



EFF SN1223 AND ON



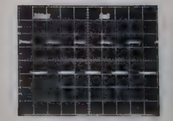
Low Loop Synthesizer PC Board (Rev C)

FM/AM 1200 FREQ SETTING	LOW LOOP OUTPUT FREQ	TUNE VOLTAGE TP 4201
0.0000	79.30000	6.00 VDC ± .5 V
1.0000	78.30000	4.50 VDC ± .5 V
1.9999	77.30010	3.00 VDC ± .5 V

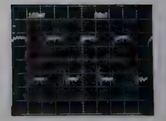
NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 4200 (E.G., R1 IS R4201).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. SN1001 THRU SN1222, R17 IS 100 K.
4. SN1001 THRU SN1287, R16 IS 47Ω.
5. SN1223 AND ON, R39 NOT USED.
6. SN1001 THRU SN1222, U14B, PIN 4 GOES DIRECTLY TO -12 V. R40 AND CR7 NOT USED.
7. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
8. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
9. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

1



2



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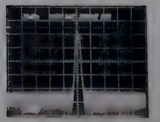

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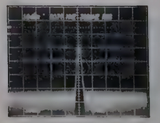


NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200 FREQUENCY SET ON 150.2 MHz USING AN X10 PROBE.

Figure 7-19 Low Loop Module (Sheet 1 of 2) (0000-5214-200-H)

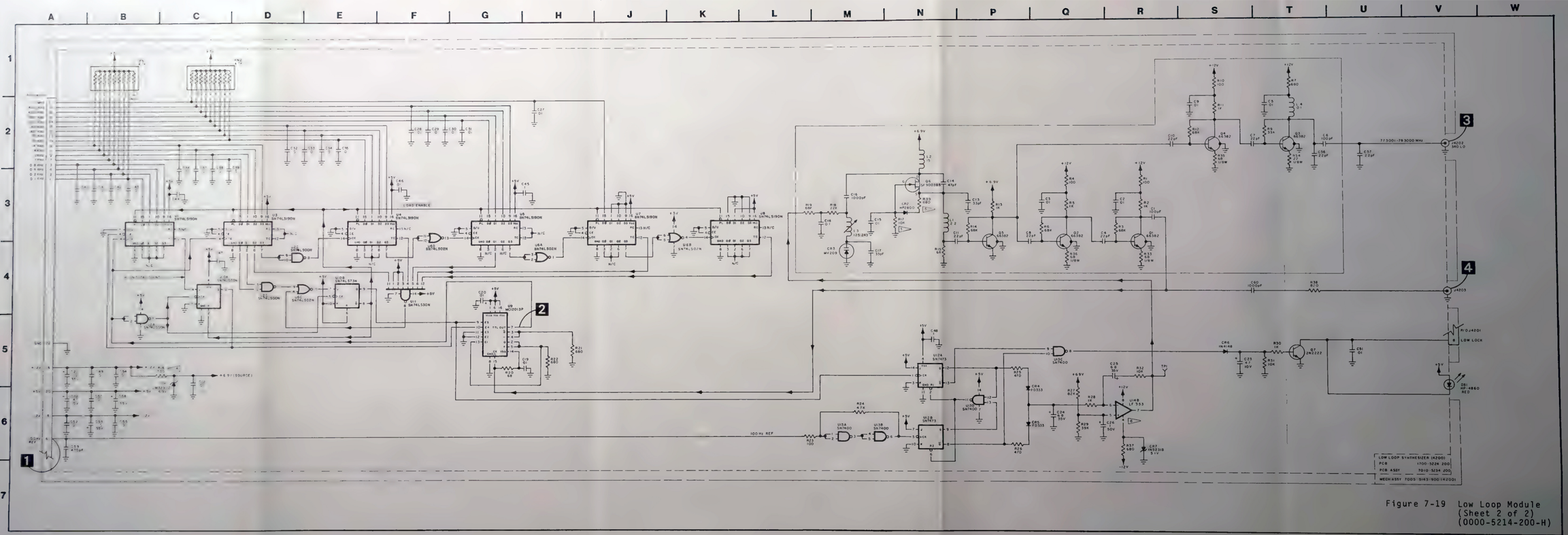
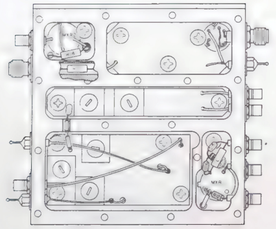
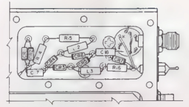
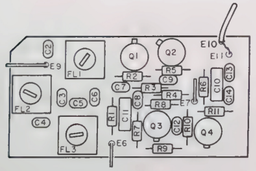


Figure 7-19 Low Loop Module (Sheet 2 of 2) (0000-5214-200-H)



IF Block Assembly (Rev J)

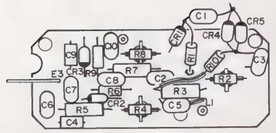


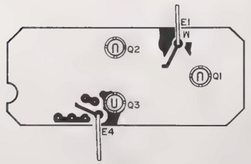


IF Amp PC Board (Rev C-2)

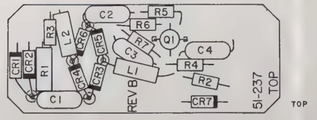


IF Mixer PC Board (Rev A)





1300 MHz Amp PC Board (Rev B)



TOP



BOTTOM

IF Voltage Protect PC Board (Rev B-1)

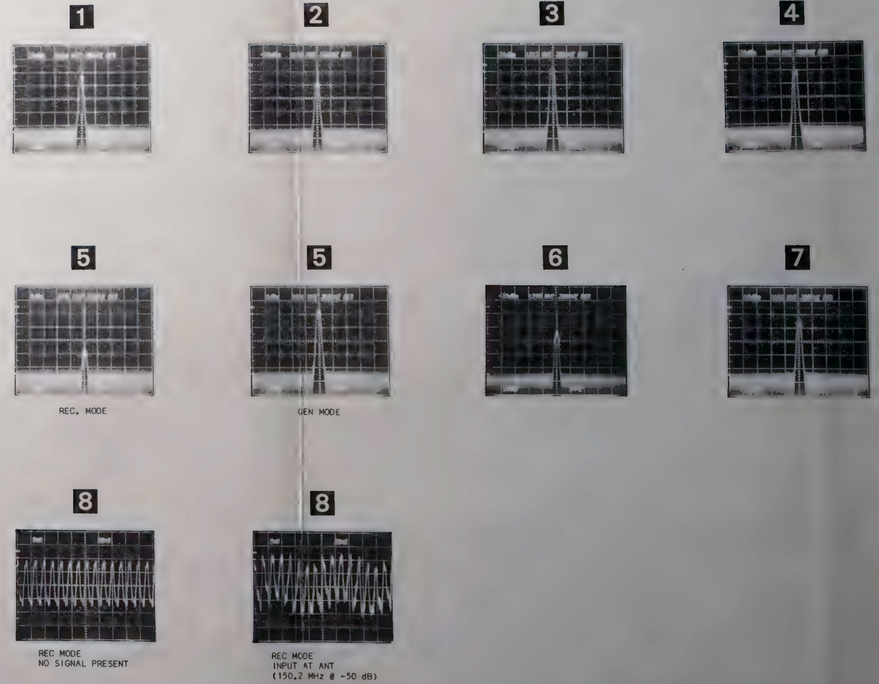


Figure 7-20 IF Block Assembly
(Sheet 1 of 2)
(0000-5111-900-H1)

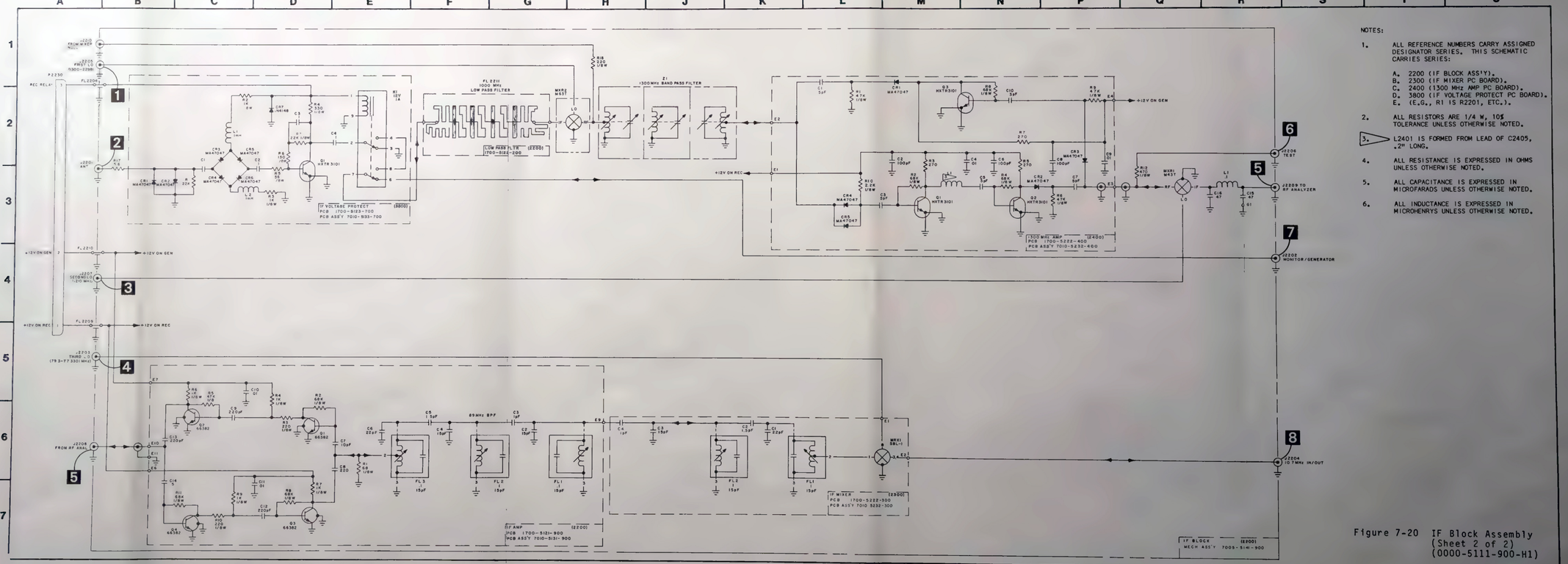
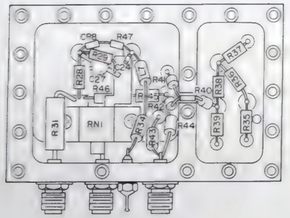
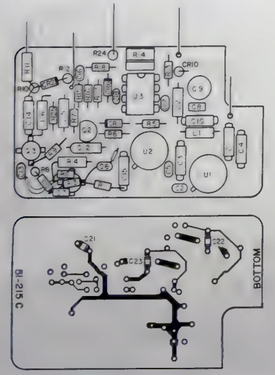


Figure 7-20 IF Block Assembly (Sheet 2 of 2) (0000-5111-900-H1)

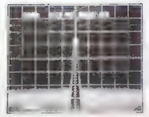


Output Amplifier Block Enclosure (Rev J)



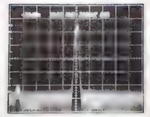
Output Amplifier PC Board (Rev C-3)

1



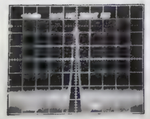
GEN MODE ONLY

2

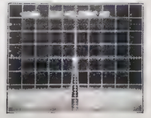


DUPLEX MODE ONLY
(150.2 MHz WITH +2 MHz OFFSET)

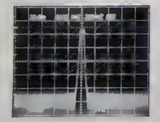
3



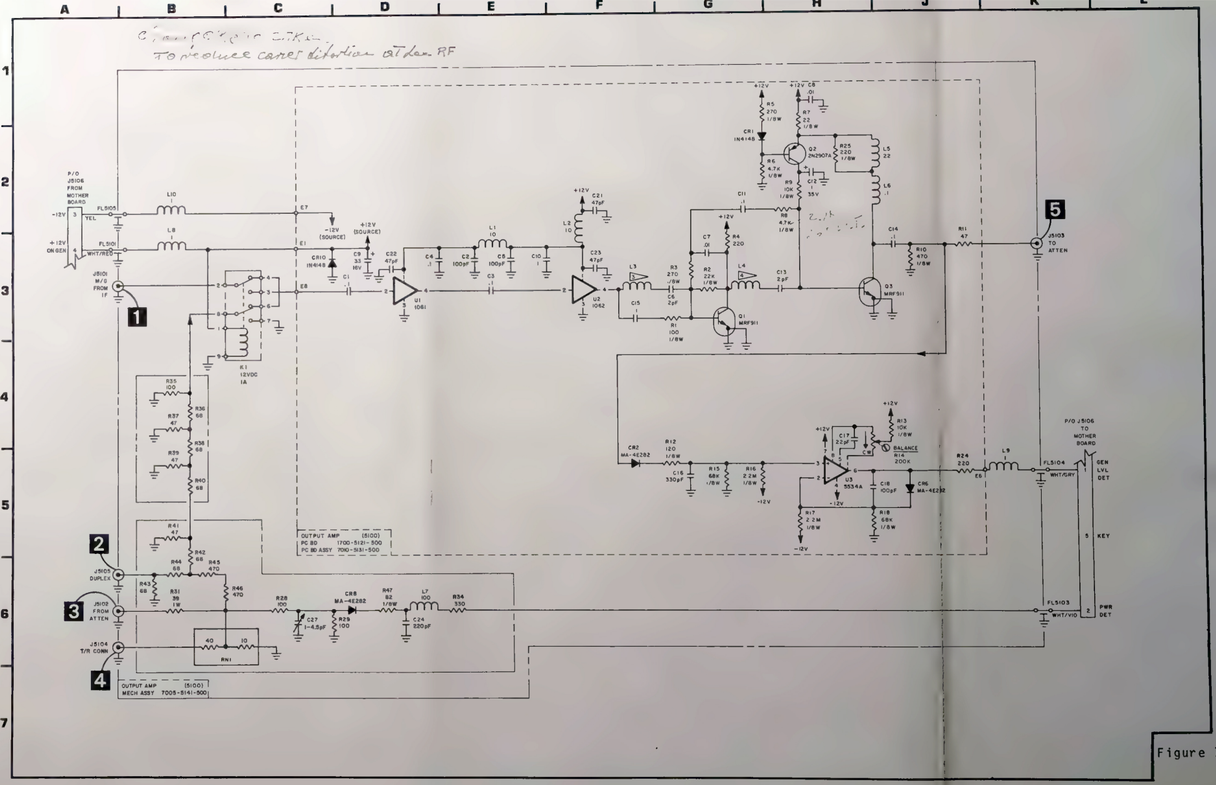
4



5



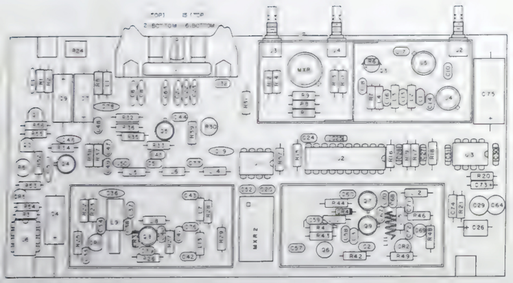
NOTE: UNLESS OTHERWISE NOTED ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200 IN GEN OR DUP GEN MODE AT A FREQUENCY OF 150.2 MHz @ -50 dBm WITH A +2 MHz OFFSET.



NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 5100 (E.G., R1 IS R5101).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. L3 IS FORMED BY THE LEAD OF C5106 CUT TO A LENGTH OF .4 INCHES.
4. L4 IS FORMED BY THE LEAD OF C5113 CUT TO A LENGTH OF .4 INCHES.
5. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
6. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
7. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

Figure 7-21 Output Amplifier Module (0000-5111-500-C3)

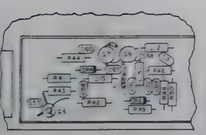




BOTTOM VIEW



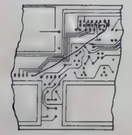
TOP VIEW
REV A, B & C



TOP VIEW
REV B ONLY



BOTTOM VIEW



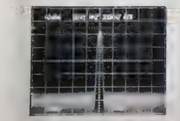
BOTTOM VIEW
REV D ONLY

Duplex PC Board (Rev F-5)

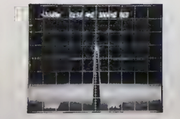
NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 1200 (E.G., R1 IS R1201).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED. PRECISION RESISTORS (1%) ARE DESIGNATED BY AN ASTERISK (*).
3. L11 IS FORMED BY A 2.4" LENGTH OF 24 GA WIRE WRAPPED 4 TURNS WITH A .125" ID.
4. R8 IS SELECTED AT TEST (SAT). NOMINAL IS 1.8 K. RANGE IS 820 TO 2.7 K.
5. SN1001 THRU SN1287, C70 IS 10 pF, C3 AND C60 IS 1800 pF, C59 NOT USED AND R41 IS 82 OHMS.
6. SN1001 THRU SN1972, R18 AND R19 IS 68 K, R20 IS 1 K AND C74 IS 2.2 µf, 25 V.
7. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
8. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
9. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

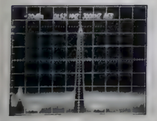
1



2



3



NOTE: ALL MEASUREMENTS WERE TAKEN WITH FM/AM-1200 IN DUPLEX MODE AT A FREQUENCY OF 150.2 MHz WITH +2 MHz OFFSET.

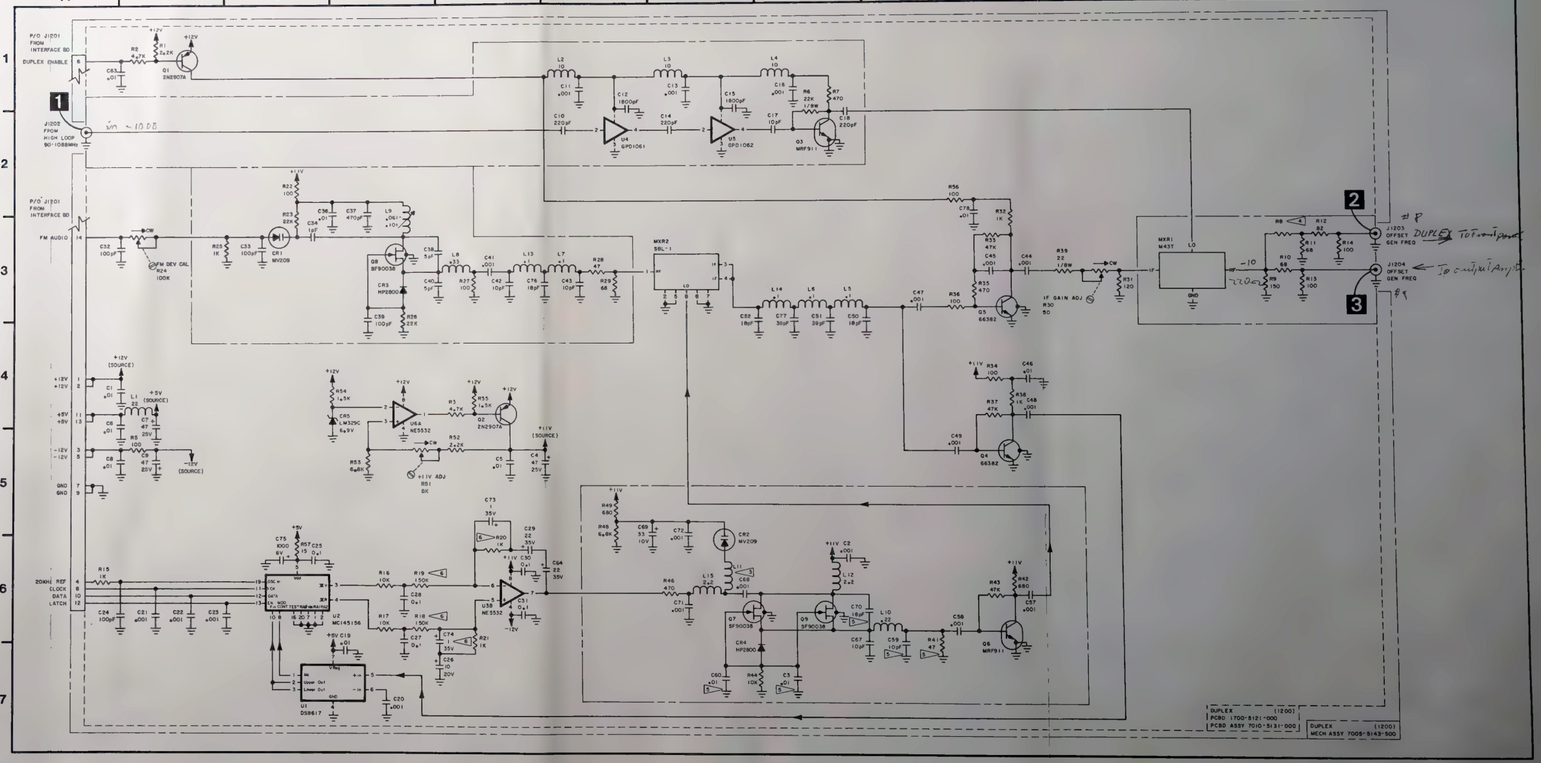
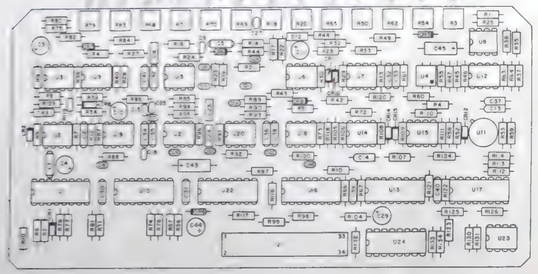


Figure 7-22 Duplex Module (0000-5113-500-F5)





Receive Audio PC Board (Rev E)

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 3300 AND 3400 (E.G., R1 IS R3301 AND R101 IS R3401).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

METER SELECT CODING													
J3301		S3704 MODULATION METER CONTROL POSITION											
		KHz/$KHz								MP		WA	
PIN #	IDENTIFIER	2	4	20	60	BATT TEST	SIG	DIST	SINAD	150	15	150	15
15	MOD MTR A	0	1	0	0	0	1	1	1	0	1	0	1
21	MOD MTR B	0	1	1	1	0	0	1	1	1	0	1	0
23	MOD MTR C	0	0	0	0	0	0	1	1	1	1	1	1
28	ONE FUNCT	0	0	0	1	0	0	1	0	0	0	0	0
30	AVG/PEAK	0	0	0	0	0	0	1	1	0	0	1	1
1 = +12 VDC 0 = 0 VDC													

J3301	REMARKS
PIN 3	+5 VDC WHEN FUNCTION GENERATOR IS SET ON ANY TONE BELOW 409.6 Hz
PIN 8	+12 VDC ON SSB AND ALL AM MODES
PIN 12	+12 VDC ON FM WIDE ONLY

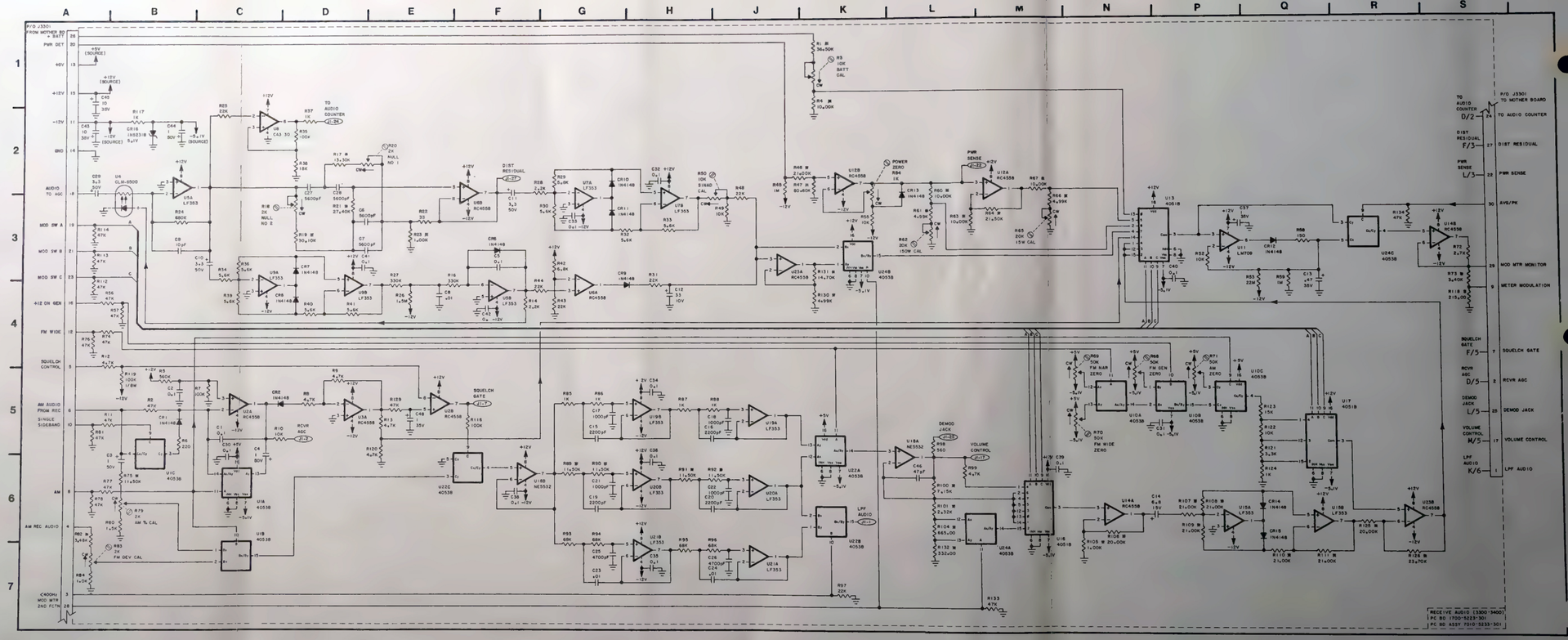
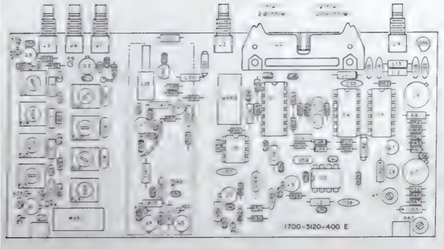
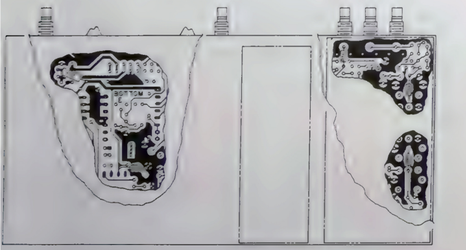


Figure 7-23 Receive Audio PC Board Assembly (0000-5213-301-D1)





BOTTOM VIEW REV C ONLY



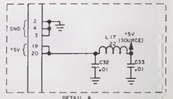
Analyzer RF PC Board (Rev F-2)

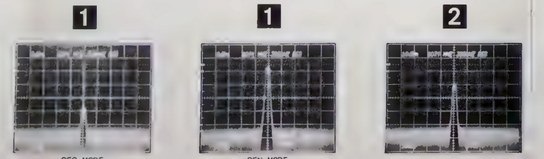
NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 400 (E.G., R1 IS R401).
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. R64 IS SELECTED AT TEST (SAT). NOMINAL IS 1.2 K. RANGE IS 1.0 K TO 2.2 K.
5. SN1001 THRU SN1286, R34 is 68Ω, R65 NOT USED, SN1287 & ON R34 IS NOT USED, AND R65 IS 56Ω.
6. SN1001 THRU SN1196, C59 IS NOT USED.
7. SN1001 THRU SN1747 R53 IS 10Ω, SN1748 & ON R53 IS 33Ω.
8. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
9. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

HORIZONTAL SWEEP SELECTOR POSITION	PIN #		
	5	7	9
1 MHz/DIV	1	0	0
2 MHz/DIV	1	0	0
5 MHz/DIV	0	1	0
10 MHz/DIV	0	1	0
20 MHz/DIV	0	1	0
50 MHz/DIV	0	0	1
.1 MHz/DIV	0	0	1
.2 MHz/DIV	0	0	1
.5 MHz/DIV	0	0	1
1 MHz/DIV	0	0	1

1 = +12 VDC 0 = 8 VDC





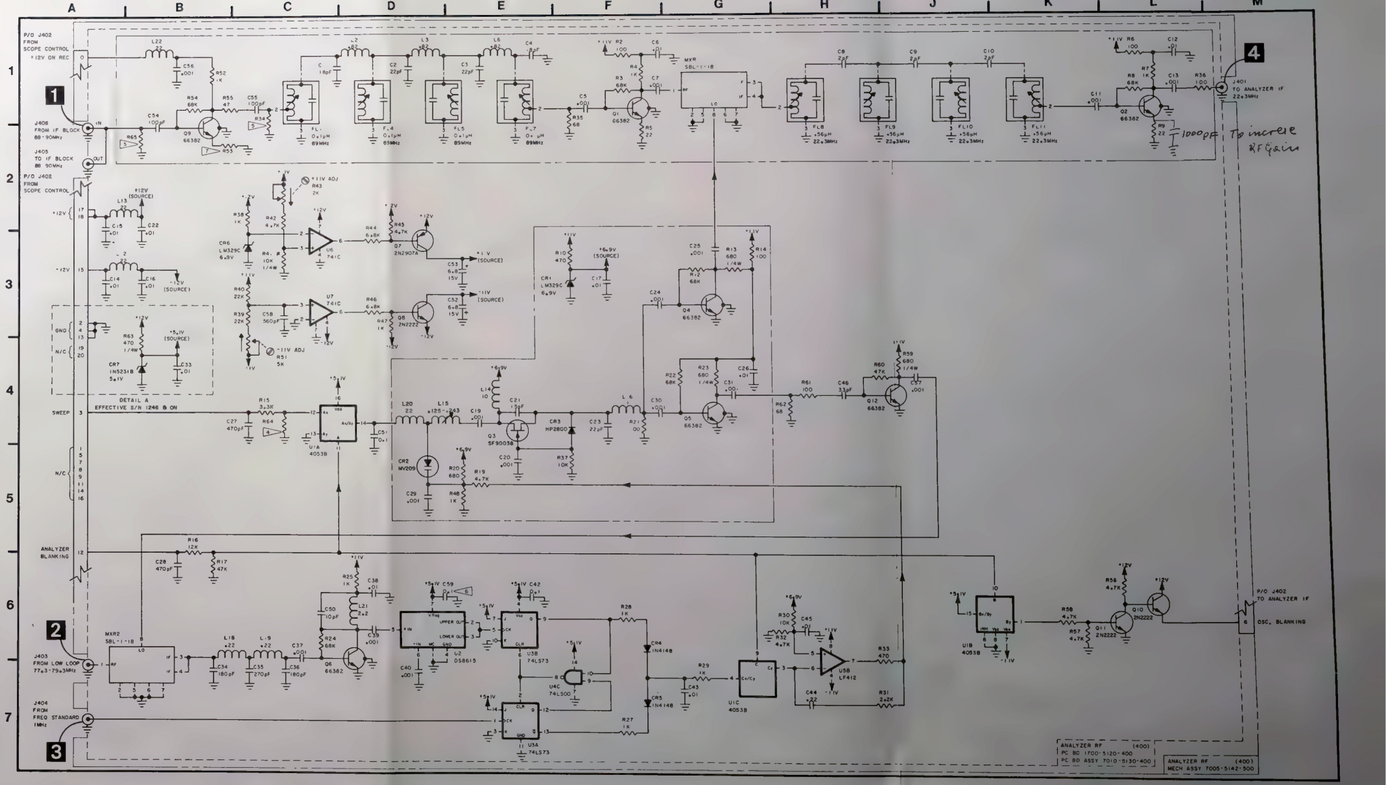
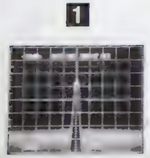
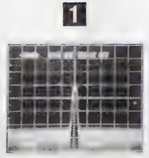


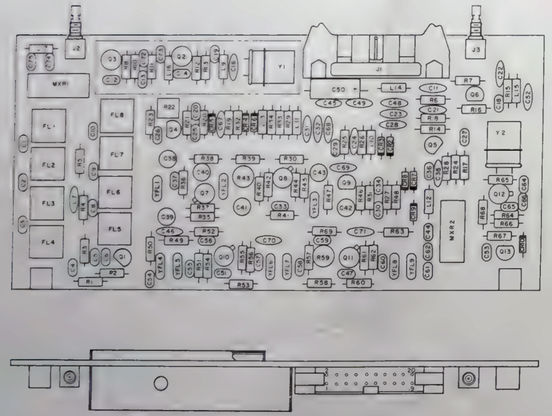
Figure 7-24 Analyzer RF Module (0000-5112-500-F)



REC MODE



GEN MODE



Analyzer IF PC Board (Rev D-7)

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 500 (E.G., R1 IS R501).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. SN1001 THRU SN1195, R42 IS 1 K, 1/4 W, 5% TOLERANCE.
4. SN1001 THRU SN1872, Q1, Q4, Q5, Q6, Q9 AND Q13 ARE 66382 TRANSISTORS. R50 IS 100Ω, 1/4 W, 5% TOLERANCE AND R54 IS 1 K, 1/4 W, 5% TOLERANCE.
5. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
6. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
7. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

HORIZONTAL SWEEP SELECTOR POSITION	PIN #		
	5	7	9
1 kHz/DIV	1	0	0
2 kHz/DIV	1	0	0
5 kHz/DIV	0	1	0
10 kHz/DIV	0	1	0
20 kHz/DIV	0	1	0
50 kHz/DIV	0	0	1
.1 MHz/DIV	0	0	1
.2 MHz/DIV	0	0	1
.5 MHz/DIV	0	0	1
1 MHz/DIV	0	0	1
1 = +12 VDC	0 = 0 VDC		

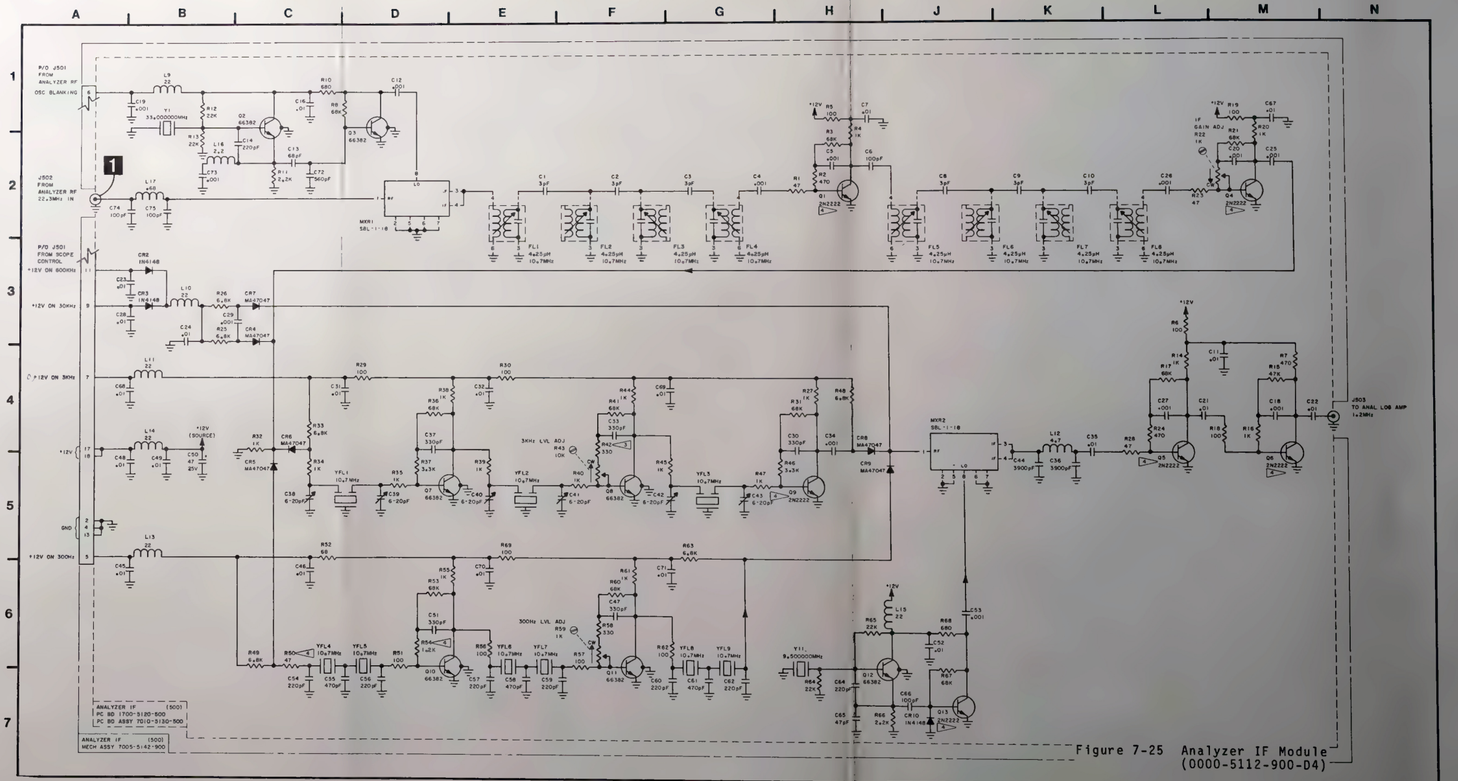
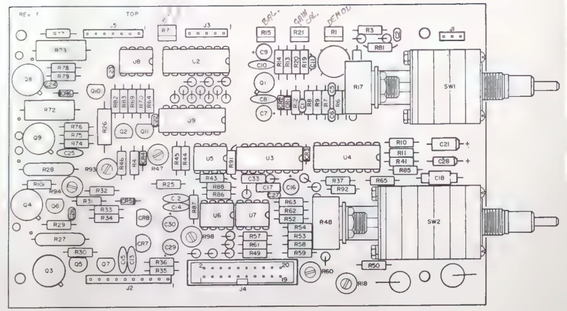
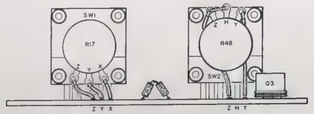
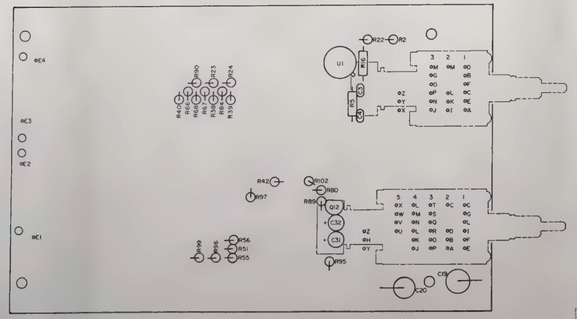


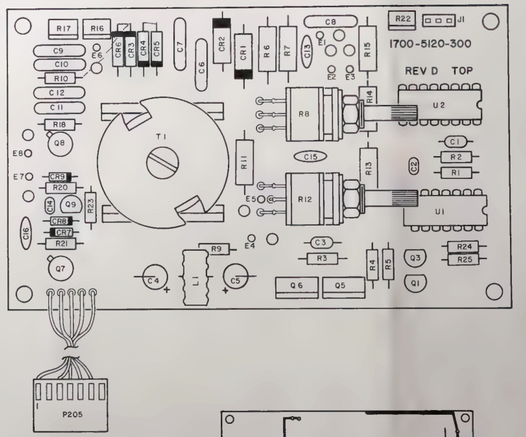
Figure 7-25 Analyzer IF Module (0000-5112-900-D4)

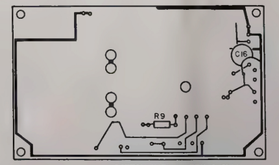






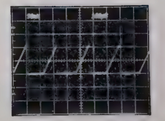
Scope Control PC Board (Rev F-4)



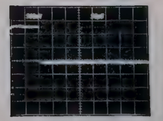


Scope Power PC Board (Rev D-6)

1



2



NOTE: ALL MEASUREMENTS WERE TAKEN WITH NO SIGNAL PRESENT, FM/AM-1200 SETTINGS: .01 mS/DIV, SQUELCH FULLY CW.

VERTICAL ATTENUATOR SELECTOR POSITION		PINS SHORTED		
		SECTION 1	SECTION 2	SECTION 3
kHz/$X10	OFF			P-Q
	.5	D-B	M-I	
	.2	D-A	M-I	
	5	B-E		M-J
	20	E-A		M-J
V/DIV	10	F-C	M-L	P-Q
	1	F-C	M-K	P-Q
	.1	C-E		M-J P-Q
	.01	D-C	M-I	P-Q
RESID				M-N P-Q

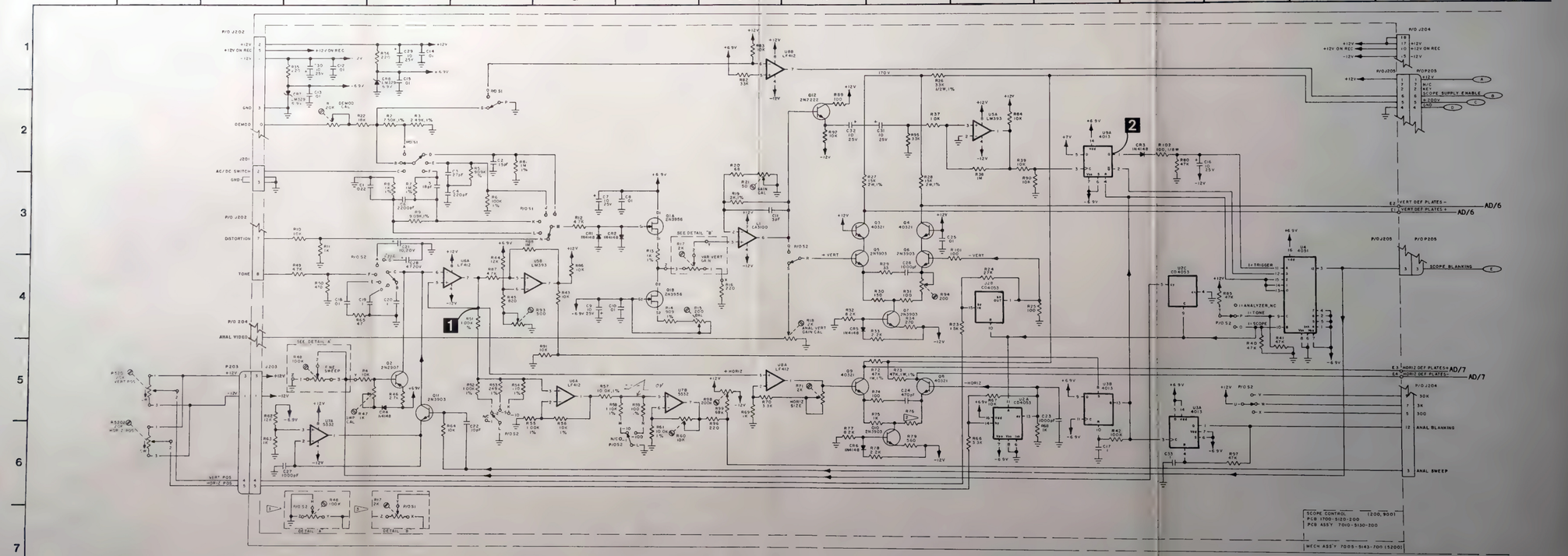
VERTICAL ATTENUATOR SELECTOR CONTROL (S201) TRUTH TABLE

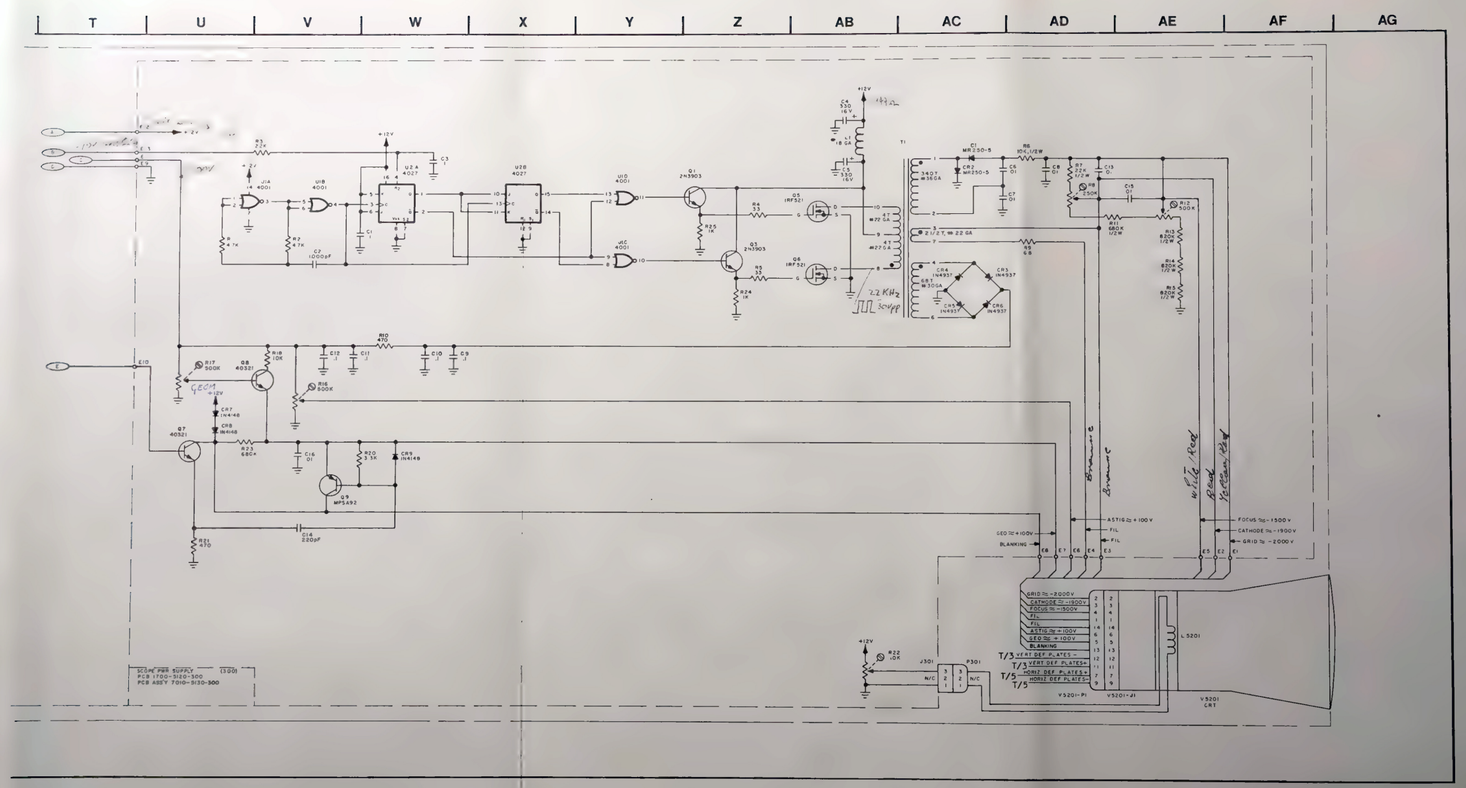
HORIZONTAL SWEEP SELECTOR POSITION		PINS SHORTED				
		SECTION 1	SECTION 2	SECTION 3	SECTION 4*	SECTION 5
	TONE	C-F		T-P, R-Q		
mS/DIV	10		C-A	T-O, R-Q		
	1		C-B	T-O, R-Q		
	.1		C-D	T-O, R-Q		
	.01	C-E		T-O, R-Q		
MHz/DIV	1	C-G		R-S		U-V
	.5	C-G, L-I		R-S		U-V
	.2	C-G		R-S	L-J	U-V
	.1	C-G		R-S	L-K	U-V
kHz/DIV	50	C-G, L-I		R-S	L-M	U-V
	20	C-G		R-S	L-J, L-M	U-W
	10	C-G		R-S	L-K, L-M	U-W
	5	C-G, L-I		R-S	L-N	U-W
	2		C-A	R-S	L-J, L-N	U-X
	1		C-A	R-S	L-K, L-N	U-X

* - SECTION 4 CONTAINS TWO "L" PINS WHICH ARE TIED TO GROUND

HORIZONTAL SWEEP SELECTOR CONTROL (S202) TRUTH TABLE

Figure 7-26 Scope Power and Control Assembly
(Sheet 1 of 3)
(0000-5110-200-F2)
(0000-5110-300-D1)


A
B
C
D
E
F
G
H
J
K
L
M
N
P
Q
R
S
T
1
2
3
4
5
6
7
P/O J202
+12V
+12V ON REC
-12V
GND
DEMOD
J201
AC/DC SWITCH
GND
P/O J202
DISTORTION
TONE
P/O J204
ANAL VIDEO
P203
J203
VERT POS
HORIZ POS
SEE DETAIL A
SEE DETAIL B
DETAIL A
DETAIL B
P/O S1
P/O S2
P/O S3
P/O S4
P/O S5
P/O S6
P/O S7
P/O S8
P/O S9
P/O S10
P/O S11
P/O S12
P/O S13
P/O S14
P/O S15
P/O S16
P/O S17
P/O S18
P/O S19
P/O S20
P/O



STANDARDS:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES:

   A. 200, 900 (SCOPE CONTROL PC BOARD).
   B. 300 (SCOPE POWER SUPPLY PC BOARD).
   C. 5200 (MECHANICAL ASSY).
   D. (E.G., R1 IS R201, ETC.)

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.

5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.

NOTES: (SCOPE CONTROL PC BOARD)

1. NOT USED.

2. R76 IS SELECTED AT TEST (SAT). NOMINAL IS 1 K. RANGE IS 800Ω TO 1.2 K.

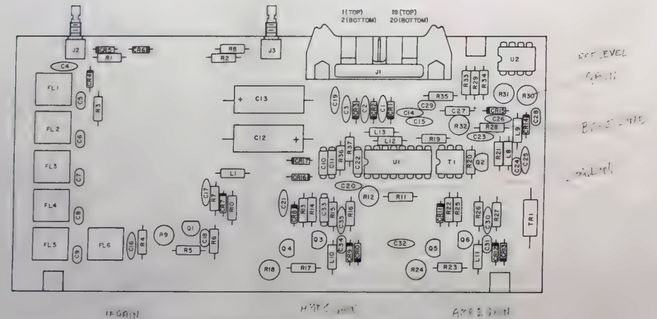
3. THESE DETAILS ARE EFFECTIVE THROUGH SN1378.

Figure 7-26 Scope Power and Control Assembly (Sheet 3 of 3) (0000-5110-200-F2) (0000-5110-300-D1)



BOTTOM VIEW

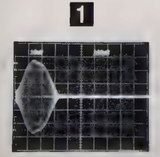
HORIZONTAL SWEEP SELECTOR POSITION	PIN #		
	5	7	9
1 kHz/DIV	1	0	0
2 kHz/DIV	1	0	0
5 kHz/DIV	0	1	0
10 kHz/DIV	0	1	0
20 kHz/DIV	0	1	0
50 kHz/DIV	0	0	1
.1 MHz/DIV	0	0	1
.2 MHz/DIV	0	0	1
.5 MHz/DIV	0	0	1
1 MHz/DIV	0	0	1
1 = +12 VDC	0 = 0 VDC		



Analyzer Log Amplifier PC Board (Rev B-7)

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 800 (E.G., R1 IS R801).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED. PRECISION RESISTORS (1%) ARE DESIGNATED BY AN ASTERISK (*).
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. SN1001 THRU SN1872, Q1 IS A 66382 WITH CASE GROUNDED.
5. R21 IS SELECT AT TEST (SAT). NOMINAL IS 1.8 K. RANGE IS 1.0 K TO 3.3 K.
6. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
7. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.



NOTE: MEASUREMENT WAS TAKEN WITH AN INPUT AT THE ANT OF 150.2 MHz @ -50 dBm USING AN X10 PROBE. FM/AM-1200 SETTING IS 1 MHz/DIV.

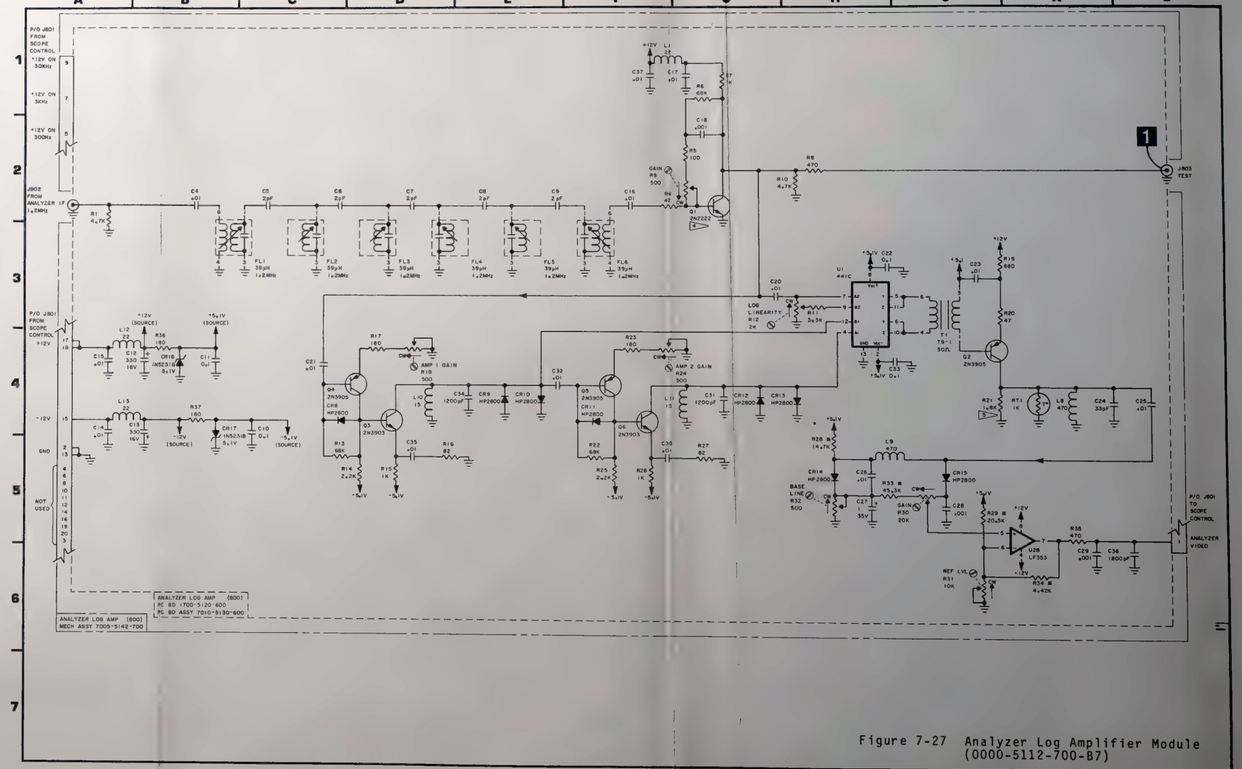
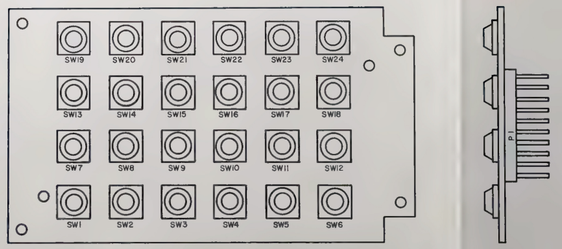


Figure 7-27 Analyzer Log Amplifier Module (0000-5112-700-B7)



Keyboard PC Board (Rev E-3)

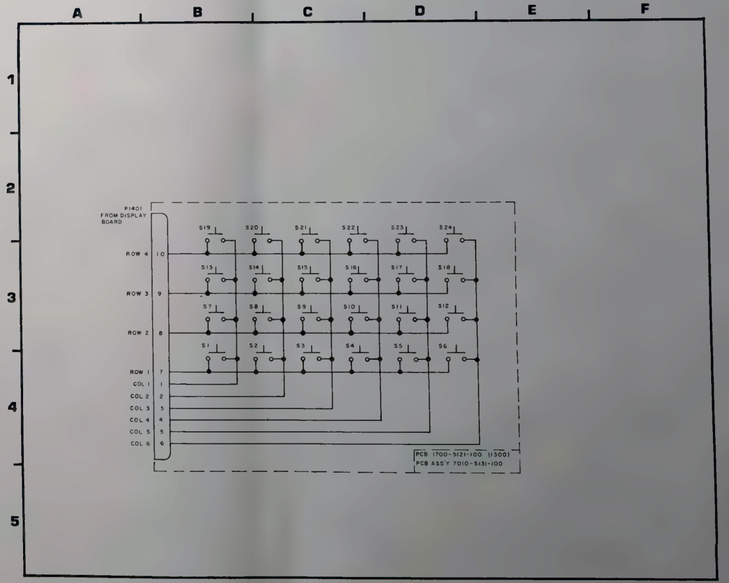
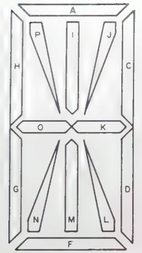


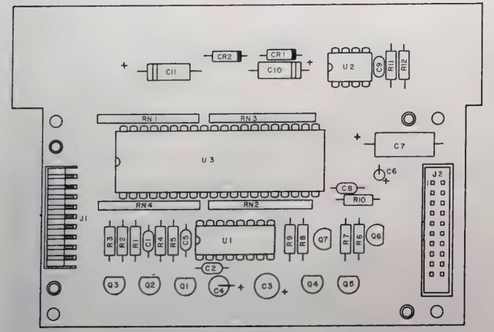
Figure 7-28 Keyboard Assembly (0000-5111-100-A)



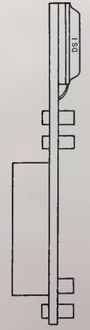
VFD DISPLAY WITH SEGMENT LOCATIONS IDENTIFIED (A THRU P)

NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 1400 (E.G., R1 IS R1401).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.
5. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.



Display PC Board (Rev D-4)



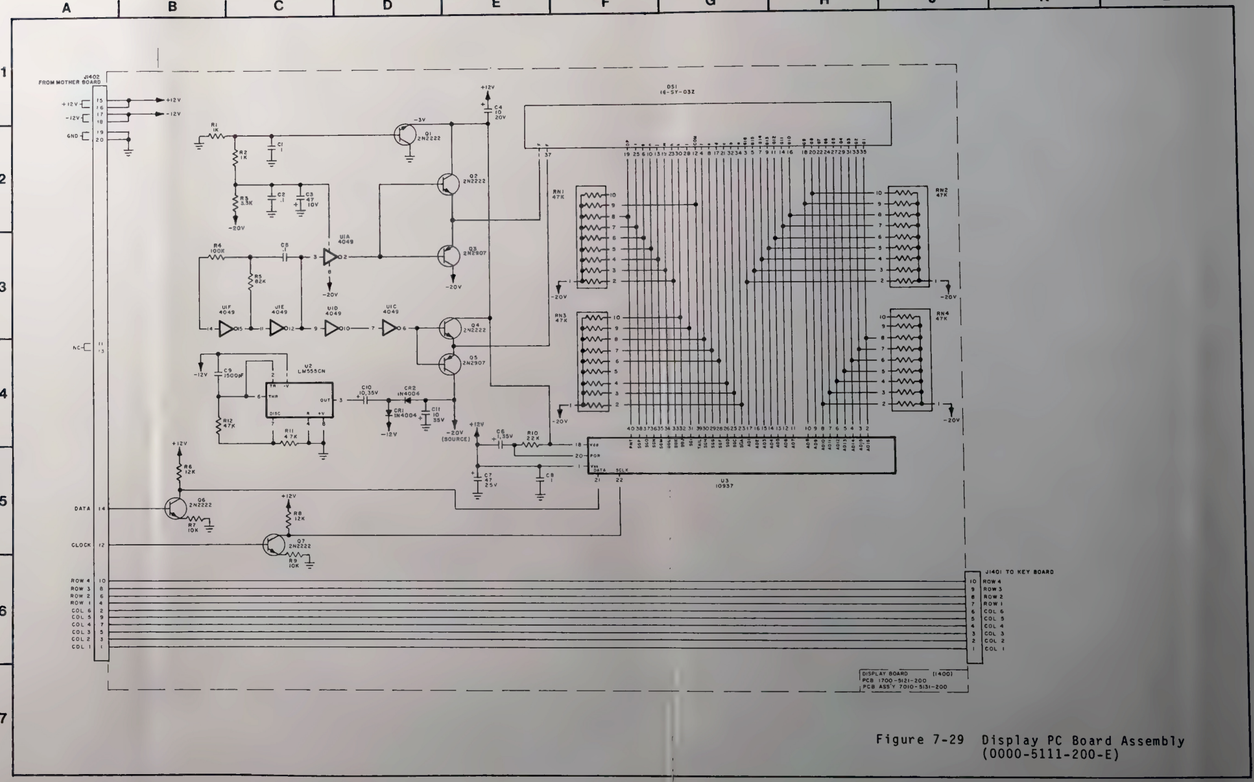
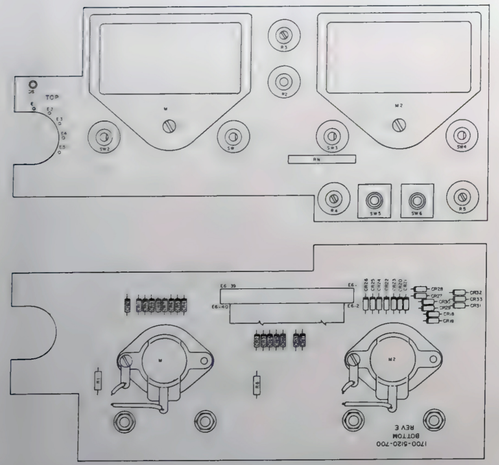


Figure 7-29 Display PC Board Assembly (0000-5111-200-E)



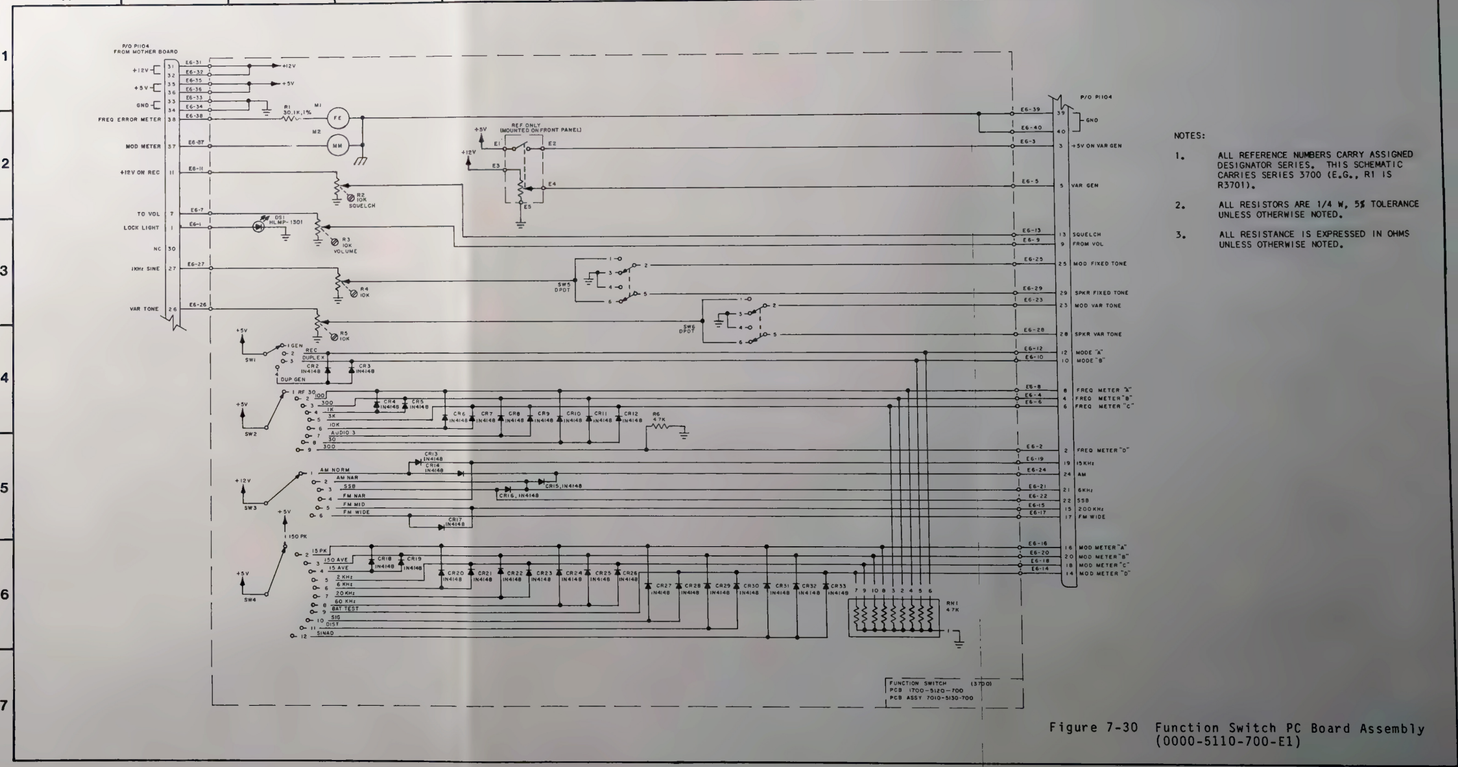
Display PC Board (Rev D-4)

S3701 MODE SELECTOR CONTROL		
POSITION	CONTROL LINES	
	MODE A	MODE B
GEN	0	0
REC	1	0
DUP	0	1
DUP/GEN	1	1
1 = +5 VDC	0 = 0 VDC	

S3703 MODULATION SELECT CONTROL						
POSITION	CONTROL LINES					
	AM	SSB	FM WIDE	6K	15K	200K
AM NORM	1	0	0	0	1	0
AM NAR	1	0	0	1	0	0
SSB	1	1	0	1	0	0
FM NAR	0	0	0	0	1	0
FM MID	0	0	0	0	0	1
FM WIDE	1	0	1	0	0	1
1 = +12 VDC				0 = 0 VDC		

S3702 FREQ ERROR METER RANGE SELECTOR CONTROL				
POSITION	CONTROL LINES			
RF	FREQ MTR A	FREQ MTR B	FREQ MTR C	FREQ MTR D
30	0	0	0	0
100	1	0	0	0
300	0	1	0	0
1K	1	1	0	0
3K	0	0	1	0
10K	1	0	1	0
AUDIO				
3	0	1	1	0
30	1	1	1	0
300	0	0	0	1
1 = +5 VDC			0 = 0 VDC	

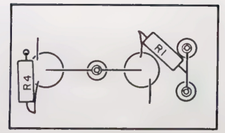
S3704 MODULATION METER CONTROL				
POSITION	CONTROL LINES			
	MOD MTR A	MOD MTR B	MOD MTR C	MOD MTR D
MP 150	0	0	0	0
MP 15	1	0	0	0
MA 150	0	1	0	0
MA 15	1	1	0	0
2 kHz/$X10	0	0	1	0
6 kHz/$X10	1	0	1	0
20 kHz/$X10	0	1	1	0
60 kHz/$X10	1	1	1	0
BATT	0	0	0	1
SIG	1	0	0	1
DIST	0	1	0	1
SINAD	1	1	0	1
1 = +5 VDC			0 = 0 VDC	



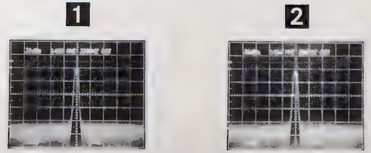
NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 3700 (E.G., R1 IS R3701).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

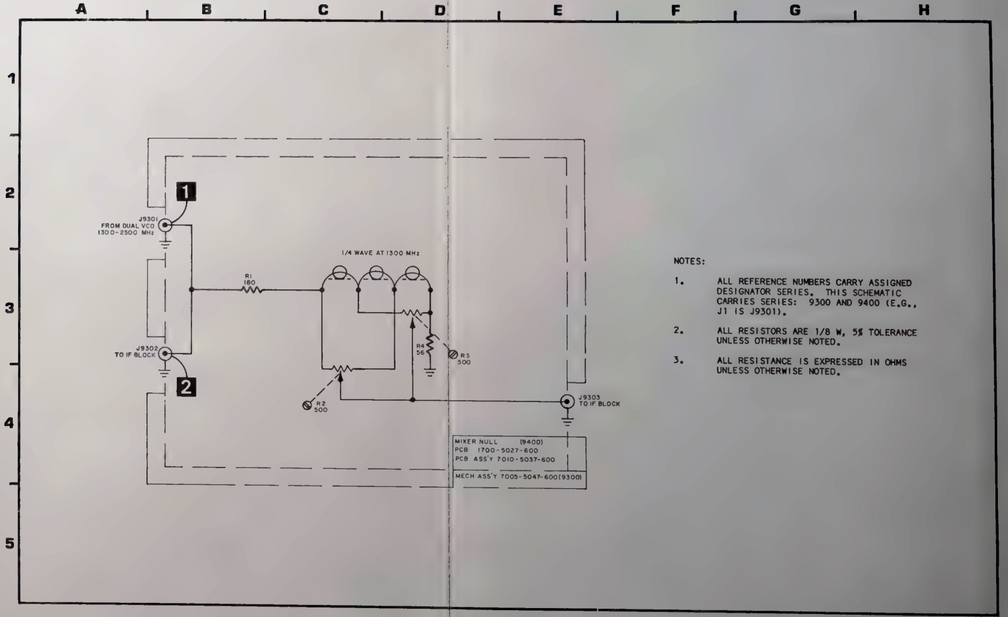
Figure 7-30 Function Switch PC Board Assembly (0000-5110-700-E1)



Null Mixer PC Board (Rev A)



NOTE: MEASUREMENTS WERE TAKEN IN GEN MODE AT A FREQUENCY OF 150.2 MHz.



NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES: 9300 AND 9400 (E.G., J1 IS J9301).
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.
3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

Figure 7-31 Null Mixer Assembly (0000-5114-700-A)



NOTES:

1. ALL REFERENCE NUMBERS CARRY ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 9000 (E.G., R1 IS R9001).

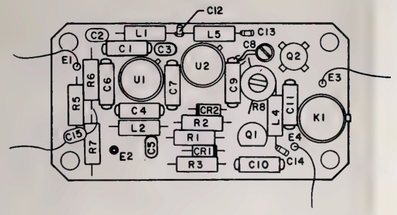
2. L3 IS FORMED FROM LEAD C8, CUT TO 2" LENGTH.

3. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE UNLESS OTHERWISE NOTED.

4. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

5. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS UNLESS OTHERWISE NOTED.

6. ALL INDUCTANCE IS EXPRESSED IN MICROHENRYS UNLESS OTHERWISE NOTED.



Generate Amplifier PC Board (Rev P-1B)

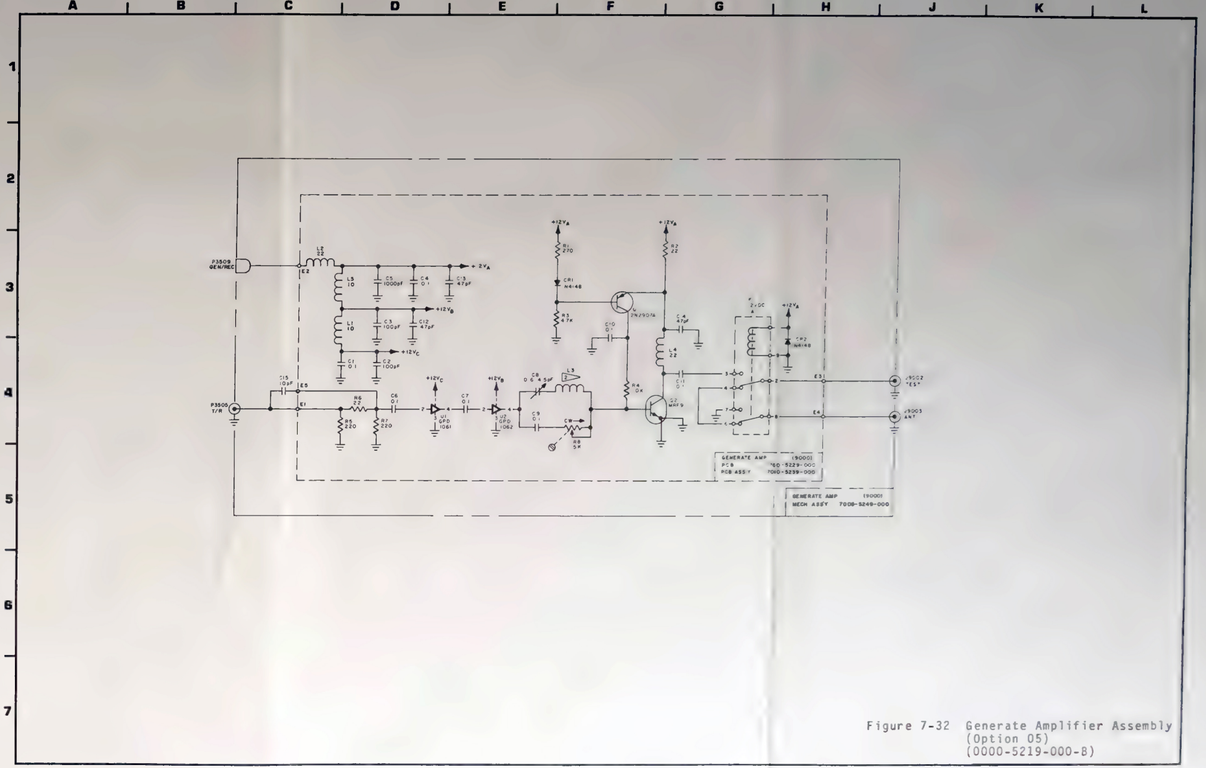


Figure 7-32 Generate Amplifier Assembly (Option 05) (0000-5219-000-B)

A-10 SPECTRUM ANALYZER

Log Scale: Within ±2 dB linearity from -30 dBm to -90 dBm indication.

Dynamic Range: 70 dB (-30 dBm to -100 dBm).

Modes:

SCAN WIDTH	BANDWIDTH
1 MHz/DIV	30 kHz
500 kHz/DIV	30 kHz
200 kHz/DIV	30 kHz
100 kHz/DIV	30 kHz
50 kHz/DIV	30 kHz
20 kHz/DIV	3 kHz
10 kHz/DIV	3 kHz
5 kHz/DIV	3 kHz
2 kHz/DIV	300 kHz
1 kHz/DIV	300 kHz

The receiver is fixed on the center frequency for monitoring while the analyzer scans as specified.

A-11 MASTER OSCILLATOR

Standard TCXO:

Accuracy: 0.5 PPM (0.50° C)

Aging: 3 PPM first year, 1 PPM per year, thereafter.

Optional TCXO: (Option 01)

Accuracy: 0.2 PPM (0-50° C)

Aging: 3 PPM first year, 1 PPM per year, thereafter.

Optional Oven: (Option 02)

Accuracy: 0.05 PPM (0-50° C)

Aging: 0.25 PPM per year.

A-12 GENERATE AMPLIFIER (Optional)

Gain:	30 ±2 dB typical, 250 kHz to 1000 MHz
Test Set Output with Amplifier Installed:	Variable to +10 dBm, FM, CW Variable to +4 dBm, AM

A-13 GENERAL CHARACTERISTICS

Dimensions:	13 1/16" wide, 7 5/16" high, 17½" deep
Weight:	32 lbs. (without options)
Temperature Range:	0 to 50° C

A-14 POWER REQUIREMENTS

Line:	105 - 130/210 - 260 VAC 50 - 400 Hz at 45 WATTS typical.
Ext. DC:	12 - 30 VDC nominal, 3 AMPS at 12 V typical, 1.4 AMPS at 28 V typical

APPENDIX B - TEST EQUIPMENT REQUIREMENTS

B-1 GENERAL

This appendix contains a list of test equipment suitable for performing all of the maintenance procedures contained in this manual. Any other equipment meeting the specifications listed in this appendix may be substituted in place of the recommended models. It should be noted that the equipment listed in this appendix may exceed the minimum required specifications for some of the procedures contained in this manual.

B-2 RECOMMENDED TEST EQUIPMENT

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Oscilloscope	Tektronix 465B	DC to 100 MHz 5 mV/div vertical trace 2 nS/div sweep rate Dual Trace
Spectrum Analyzer	Tektronix 7613 Frame Tektronix 7L13/U Spectrum Analyzer	Variable Persistance Storage Oscilloscope Frequency Range: 1 kHz to 2.5 GHz Resolution Bandwidth: 30 Hz to 3 MHz
Tracking Generator	Tektronix TM503 Frame	Three-wide Mainframe
	Tektronix TR502 Tracking Generator	Frequency Range: 100 kHz to 1.8 GHz Output Level: 0 dBm, ±0.5 dB Power Range: 0 to -59 dBm in 10 and 1 dB steps
Frequency Counter	Fluke Model 7220A	Frequency Range: 5 Hz to 1300 MHz
Digital Multimeter	Fluke Model 8010A	3½ digit, ±0.1% basic DC accuracy
Distortion Analyzer	Sound Technology Model 1700B	Frequency Range: 10 Hz to 110 kHz Accuracy: .002% distortion AC Voltage Accuracy: 2%

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Function Generator	Wavetek 182A	Frequency Range: .004 Hz to 4 MHz Functions: Sine, Triangle & Square High Level Output: 20 Vp-p (10 Vp-p into 50Ω)
Signal Generator	Hewlett Packard 8640B	Frequency Range: 1 to 1000 MHz Resolution: 0.1 to 100 Hz Accuracy: 2×10^{-6} RF Output: +20 to -130 dBm
Modulation Meter	Boonton Model 82AD	Frequency Range: 10 MHz to 1.2 GHz Accuracy: FM: ±2% of reading from 30 Hz to 100 kHz Accuracy: AM: ±2% of reading from 10 Hz to 90% AM and 5% of reading below 10% and above 90%; from 30 Hz to 100 kHz Resolution: 0.1% of full scale for FM and AM
RF Power Source	MCL 15122 Main Frame 6048 Oscillator Module	Frequency Range: 50 to 200 MHz Power Range: 0 to 65 W

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
RF Power Meter with Power Detector	Boonton RF Microwatt-meter Model 42 BD	Frequency Range: 200 kHz to 18 GHz Power Range: 1.0 nW to 10 mW Accuracy: ±0.25% fs ±0.15 dB >10 nW
	Boonton Power Sensor Model 41-4A	Frequency Range: 200 kHz to 7 GHz Power Range: 1 nW to 10 mW Accuracy: ±0.3 dB >10 nW
Power Supply	B&K 1601	Regulation: .1% or 1 mV Ripple: 5 mV Voltage Range: 0-50 VDC @ 0-2 A

APPENDIX C - TABLE OF USER I/O PORTS/CONNECTOR PIN OUT TABLES

C-1 TABLE OF I/O PORTS

CONNECTOR NAME	CONNECTOR TYPE	SIGNAL INPUT/OUTPUT	SIGNAL TYPE
T/R	BNC	Input/Output	RF
AUX PWR	Banana Jack	Output	+12 VDC
DUPLEX Output	BNC	Output	RF
EXT MOD/SINAD	BNC	Input/Output	Audio
DEMOD	BNC	Output	Audio
TONE OUT	BNC	Output	Audio
MIC/ACC	5 Pin Microphone Connector	Input/Output	See Pin Out
SCOPE	BNC	Input	DC to 1 MHz
ANT	BNC	Input	RF
RS-232	25 Pin, Type D	Input/Output	See Pin Out
External Reference	BNC	Input/Output	10 MHz RF

C-2 PIN OUT TABLE FOR MIC/ACC CONNECTOR

MIC/ACC CONNECTOR PIN ASSIGNMENTS			
Pin No.	Signal Name	Signal Type	Input/Output
1	+12 VDC	DC Voltage	1/8 AMP Fused Output
2	Chassis GND		
3	Mic Key	Switched	GND for Generate
4	Mic Audio	Audio	Input
5	Tone Key	Switched	GND to Remove Variable Tone

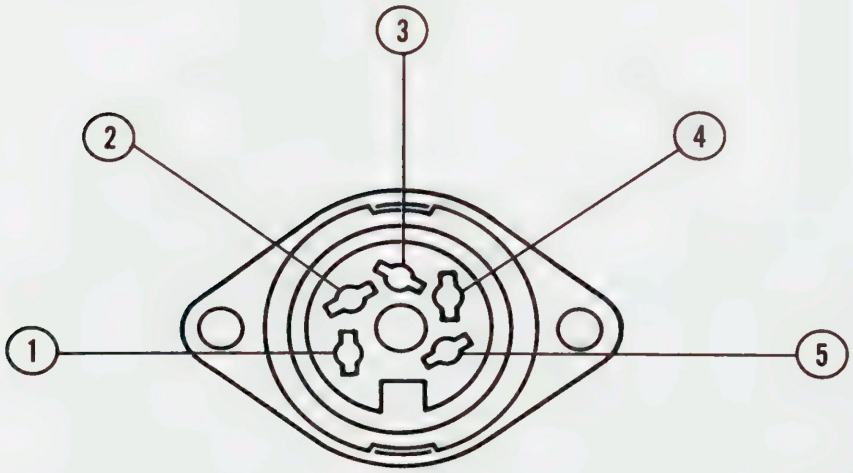


Figure C-1 MIC/ACC Connector Pin Identification (Front View)

C-3 PIN OUT TABLE FOR RS-232 CONNECTOR

RS-232 CONNECTOR PIN ASSIGNMENTS (The FM/AM-1200 is used as a terminal.)		
Pin No.	Input/Output	Remarks
2 (RXD)	← Commands	
3 (TXD)	Info →	
4 (RTS)	→	If low, FM/AM-1200 can receive command. If high FM/AM-1200 is busy.
5 (CTS)	←	If low, terminal is not ready to receive. If not used, it must be tied high.
7 (Common Ground)		
1, 6 and 8 thru 25 not used		

FM/AM-1200 PROTOCOL

No Parity

Must Be Half Duplex

Must Be Upper Case

8 Data Bits Per Character

Bit 8 Must Be Zero (Most Significant Bit)

1 Stop Bit (End Of Character)

High Level = -12V

Low Level = +12V

APPENDIX D - SPECIAL ACCESSORY TEST EQUIPMENT

D-1 GENERAL

This appendix contains recommendations for constructing special equipment necessary for performing certain test procedures in this manual.

D-2 BATTERY LOAD SIMULATOR

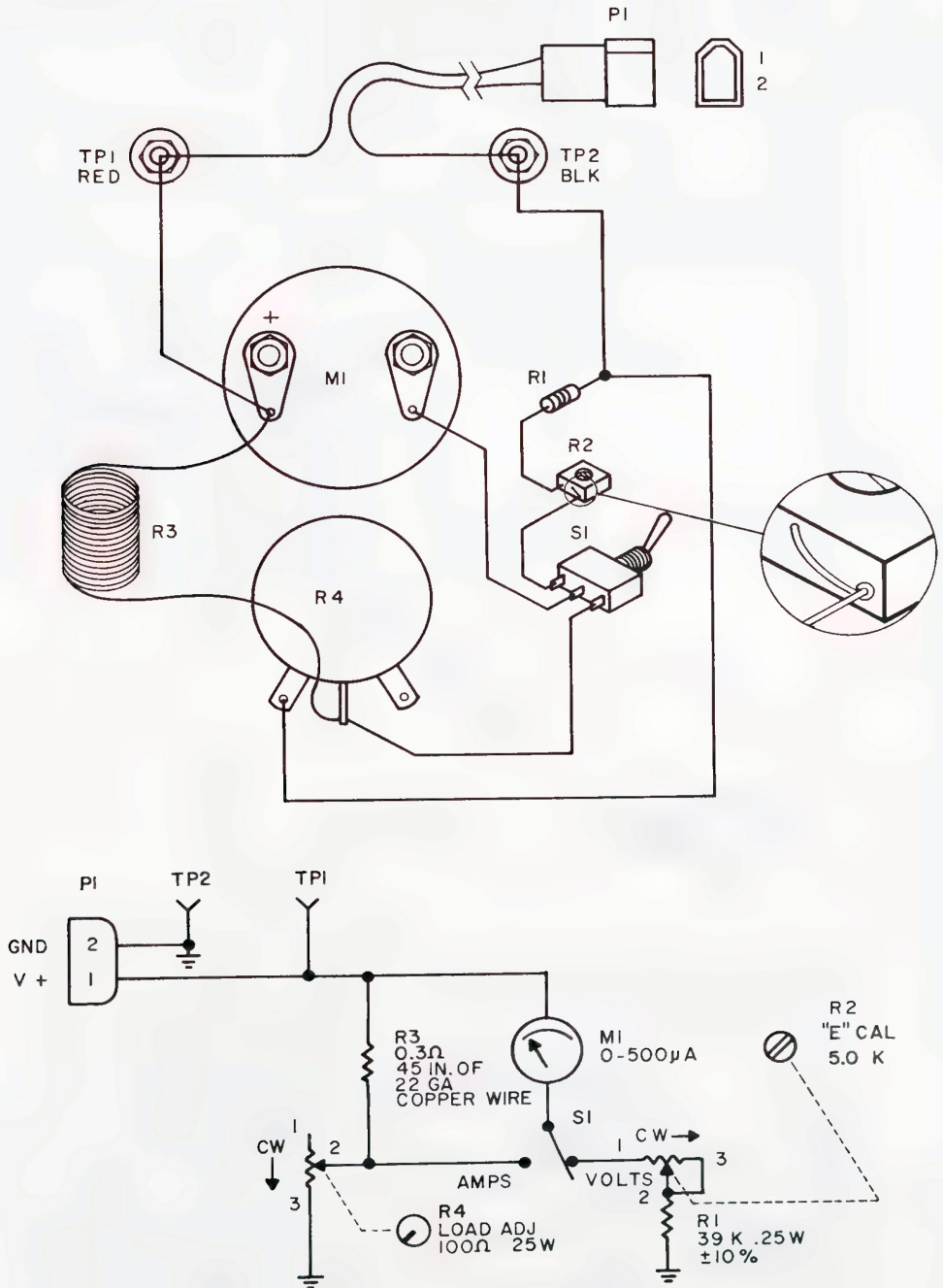
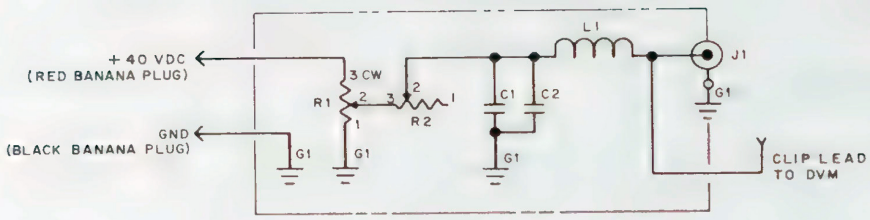
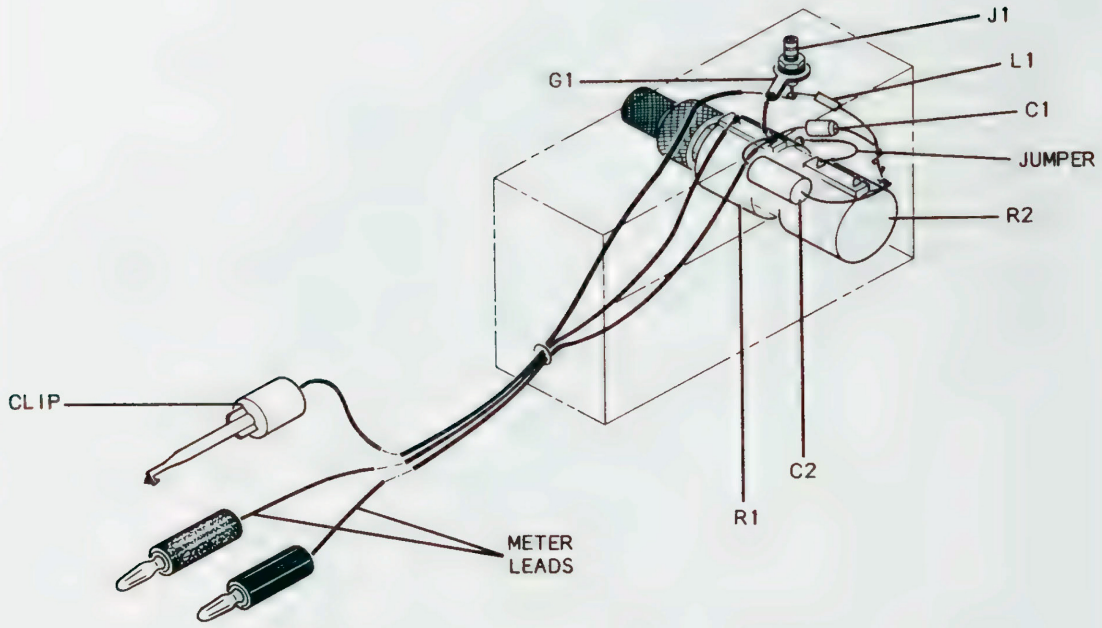


Figure D-1 Circuit Schematic and Diagram of Battery Load Simulator

D-3 TUNE CONTROL POT





PART	TYPE	IFR PART NO.
R1, R2	10K, 10 TURN, 5%	4756-0000-001
C1	4.7 µF, 35V TANT.	1502-0104-010
C2	0.1 µF, 50V POLY CARB	1507-0475-018
L1	22 µH	1801-0022-001
J1	SMB MALE	2123-0000-038
METER LEADS	ANY (RED & BLACK)	----
CLIP	ANY	----
CLIP LEAD	ANY	----
G1	GROUND LUG	----
KNOBS	ANY	----
ENCLOSURE	ANY	----

Figure D-2 Circuit Schematic and Diagram of Tune Control Pot

APPENDIX E - dBm TO MICROVOLT CONVERSION CHART

dBm	µV	dBm	µV	dBm	µV
0	224,000	-47	1,000	-94	4.47
-1	200,000	-48	891	-95	3.99
-2	178,000	-49	795	-96	3.55
-3	159,000	-50	709	-97	3.17
-4	141,000	-51	633	-98	2.82
-5	126,000	-52	563	-99	2.52
-6	112,000	-53	501	-100	2.24
-7	100,000	-54	447	-101	2.00
-8	89,100	-55	399	-102	1.78
-9	79,500	-56	355	-103	1.59
-10	70,900	-57	317	-104	1.41
-11	63,300	-58	282	-105	1.26
-12	56,300	-59	252	-106	1.12
-13	50,100	-60	224	-107	1.00
-14	44,700	-61	200	-108	0.891
-15	39,900	-62	178	-109	0.795
-16	35,500	-63	159	-110	0.709
-17	31,700	-64	141	-111	0.633
-18	28,200	-65	126	-112	0.563
-19	25,200	-66	112	-113	0.501
-20	22,400	-67	100	-114	0.447
-21	20,000	-68	89.1	-115	0.399
-22	17,800	-69	79.5	-116	0.355
-23	15,900	-70	70.9	-117	0.317
-24	14,100	-71	63.3	-118	0.282
-25	12,600	-72	56.3	-119	0.252
-26	11,200	-73	50.1	-120	0.224
-27	10,000	-74	44.7	-121	0.200
-28	8,900	-75	39.9	-122	0.178
-29	7,950	-76	35.5	-123	0.159
-30	7,090	-77	31.7	-124	0.141
-31	6,330	-78	28.2	-125	0.126
-32	5,630	-79	25.2	-126	0.112
-33	5,010	-80	22.4	-127	0.100
-34	4,470	-81	20.0	-128	0.0891
-35	3,990	-82	17.8	-129	0.0795
-36	3,550	-83	15.9	-130	0.0709
-37	3,170	-84	14.1	-131	0.0633
-38	2,820	-85	12.6	-132	0.0563
-39	2,520	-86	11.2	-133	0.0501
-40	2,240	-87	10.0	-134	0.0447
-41	2,000	-88	8.91	-135	0.0399
-42	1,780	-89	7.95	-136	0.0355
-43	1,590	-90	7.09	-137	0.0317
-44	1,410	-91	6.33	-138	0.0282
-45	1,260	-92	5.63	-139	0.0252
-46	1,120	-93	5.01	-140	0.0224

APPENDIX F - REPACKING FOR SHIPMENT

F-1 SHIPPING INFORMATION

IFR test sets returned to factory for calibration, service or repair must be repackaged and shipped subject to the following conditions:

Do not return any products to factory without first receiving authorization from IFR Customer Service Department.

CONTACT:

Customer Service Dept.
IFR, Inc.
10200 West York Street
Wichita, Kansas 67215

Telephone: (800)-835-2350
TWX: 910-741-6952

All test sets must be tagged with:

a. Owner's identification and address.
b. Nature of service or repair required.
c. Model No.
d. Serial No.

Sets must be repackaged in original shipping containers using IFR packing molds. If original shipping containers and materials are not available, contact IFR Customer Service Dept. for shipping instructions.

All freight costs on non-warranty shipments are assumed by customer. (See "Warranty Packet" for freight charge policy on warranty claims.)

F-2 REPACKING PROCEDURE (Reference - Figure F-1):

1. Make sure bottom packing mold is seated on floor of shipping container.
2. Carefully wrap test set with polyethylene sheeting to protect finish.
3. Place test set into shipping container, making sure set is securely seated in bottom packing mold.
4. Place top packing mold over top of set and press down until mold rests solidly on bottom packing mold.
5. Close shipping container lids and seal with shipping tape or an industrial stapler. Tie all sides of container with break resistant rope, twine or equivalent.

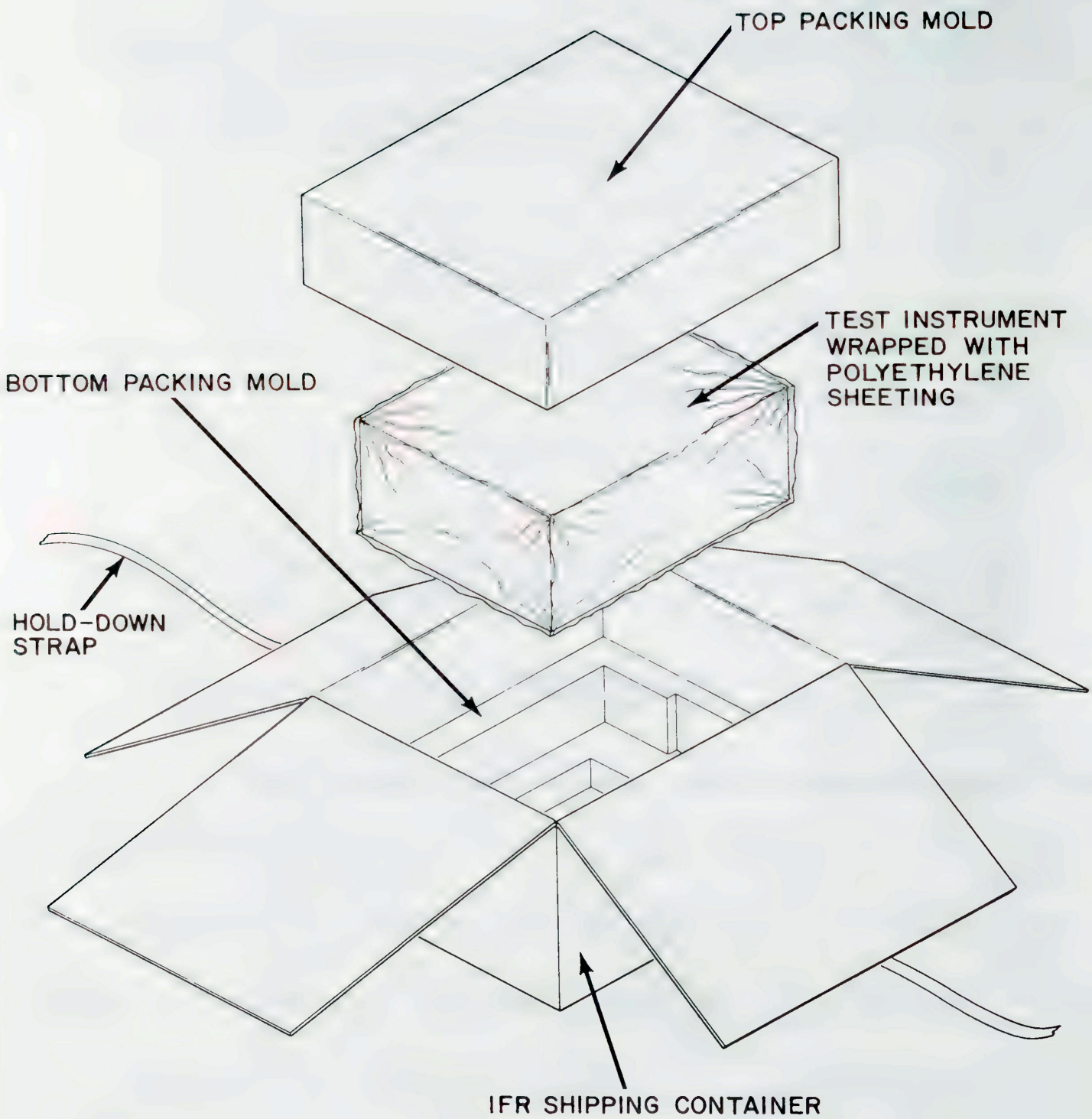


Figure F-1 Repacking for Shipment

APPENDIX G - ABBREVIATIONS & SYMBOLS

G-1 GENERAL

Defined below are various abbreviations and symbols which are commonly used throughout the FM/AM-1200 Maintenance Manual text.

G-2 GENERAL ABBREVIATIONS

A	- Ampere
AC or ac	- Alternating Current
Adj	- Adjustment
AGC	- Automatic Gain Control
AM	- Amplitude Modulation
Amp	- Ampere
ANALY DISP.	- Analyzer Dispersion
Assy	- Assembly
BATT	- Battery
BCD	- Binary Coded Decimal
BFO	- Beat Frequency Oscillator
°C	- Degrees Celsius
CAL	- Calibration
ccw	- Counterclockwise
CRT	- Cathode Ray Tube
cw	- Clockwise
CW	- Carrier Wave
DAC	- Digital to Analog Converter
dB	- decibels
dBc	- decibels above or below carrier level
dBm	- decibels above (or below) 1 milliwatt
DC or dc	- Direct Current
DCR	- Duty Cycle Regulator
DEFLEC AMP	- Deflection Amplifier
DEMOD	- Demodulation, demodulate or demodulated
DEV	- Deviation
DMM	- Digital Multimeter
DVM	- Digital Voltmeter
ECL	- Emitter Coupled Logic
EXT ACC	- External Accessory
EXT MOD	- External Modulation
EXT DC	- External Direct Current
°F	- Degrees Fahrenheit
FET	- Field Effect Transistor
FILT	- Filter
FM	- Frequency Modulation
FREQ	- Frequency
GEN	- Generate
GHz	- Gigahertz
GND	- Ground
HI LVL	- High Level
HORIZ	- Horizontal

Hz	- Hertz
IC	- Intergated Circuit
IF	- Intermediate Frequency
INT MOD	- Internal Modulation
IPC	- Illustrated Parts Catalog
Kg/cm^3	- Kilogram per cubic centimeter
kHz	- kilohertz
L/H	- Left-hand
LOG LIN	- Logarithmic Linearity
LO	- Local Oscillator
mA	- Milliamperes
MAX DISP	- Maximum Dispersion
Mech	- Mechanical
MHz	- Megahertz
MOD	- Modulation
MON	- Monitor
MTR	- Meter
µs	- microsecond
µV	- microvolt
ms or mSec	- millisecond
mV	- millivolt
mW	- milliwatt
MULT	- Multiplier
NC	- Not Connected
N/A	- Not Applicable
NORM	- Normal
OSC	- Oscillator
para	- paragraph
PC Bd	- Printed Circuit Board
PLL	- Phase Lock Loop
Preamp	- Preamplifier
psi	- pounds per square inch
PWR	- Power
PWR MON	- Power Monitor
RCVR	- Receiver
REF	- Reference
RF	- Radio Frequency
R/H	- Right-hand
RMS	- Root Mean Square
ROM	- Read Only Memory
sec	- Seconds
Scope Dev	- Oscilloscope Deviation
SIG	- Signal
SSB	- Single Sideband
SW	- Switch
TCXO	- Temperature Compensated Crystal Oscillator
TRANS	- Transmitter or Transceiver
TTL	- Transistor Transistor Logic
V	- Volts
Vp	- Volts Peak

Vp-p	- Volts Peak-to-Peak
VAC	- Volts Alternating Current
VCO	- Voltage Controlled Oscillator
VDC	- Volts Direct Current
VHF	- Very High Frequency
VOL	- Volume
VRMS	- Volts Root Mean Square
VSWR	- Voltage Standing Wave Ratio
W	- Watts
XMTR	- Transmitter
XTAL	- Crystal

G-3 ABBREVIATIONS FOR REFERENCE DESIGNATORS

BR	- Bridge Rectifier
C	- Capacitor
CR	- Diode
DS	- Display Lamps
E	- Terminal
FL	- Feed-thru Filter
G	- Ground
J	- Connector (Fixed)
K	- Relay
L	- Inductor
M	- Meter
MX	- Mixer
P	- Connector (Movable)
Q	- Transistor
R	- Resistor
SW	- Switch
T	- Transformer
TU	- Tuning Pole
U	- Integrated Circuit
VR	- Voltage Regulator
Y	- Crystal
YFL	- Crystal Filter

APPENDIX H - OPTIONAL GENERATE AMPLIFIER (OPTION 05)

H-1 GENERAL

The Generate Amplifier is a 30 dB amplifier intended to increase the output level of a generated signal above the normal maximum level by the service monitor. It is not designed to receive any signal directly from a Unit Under Test (UUT); however, if properly installed, it can be used to transmit and receive signals "off the air", using the antenna.

CAUTION

DO NOT TRANSMIT FROM A UUT DIRECTLY INTO THE GENERATE AMPLIFIER, OR THROUGH AN EXTERNAL ATTENUATOR. DAMAGE TO THE GENERATE AMPLIFIER AND/OR THE SERVICE MONITOR WILL RESULT.

H-2 INSTALLATION

Insert the banana plug on the Generate Amplifier into the AUX PWR Jack on the Front Panel of the Service Monitor and connect the BNC connector to the T/R Jack.

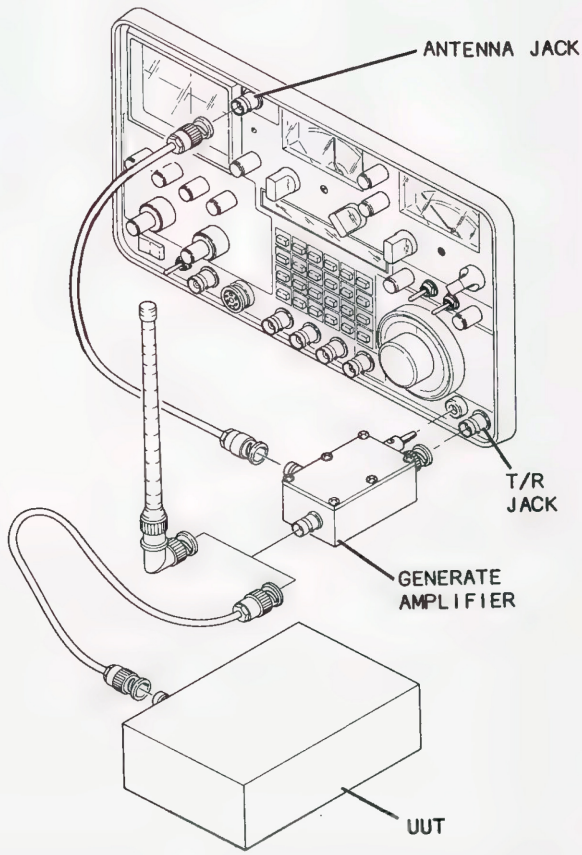
For Direct Connection To UUT:

Connect coax cable between the UUT Test Jack on the Generate Amplifier and the Microphone Jack or other audio input on the UUT.

For Radio Installation Checkout:

WARNING

THIS TEST MUST BE PERFORMED WITH THE SERVICE MONITOR AND UUT INSIDE A SHIELDED AREA TO PREVENT UNRESTRICTED RADIATION OF RF SIGNALS.



Connect coax between Antenna Jack on the Front Panel of the Service Monitor and the Antenna Jack on the Generate Amplifier. Connect accessory antenna to the UUT Test Jack on the Generate Amplifier.

H-3 OPERATION

Refer to FM/AM-1200 Operation Manual, Section 4 and perform the procedures for generating and receiving RF signals.

VERSION 1.4 * NOTE: ASTERISK (*) BELOW, MARKS E-PROM LOCATION(S) EFFECTED BY THIS UPDATE.
EFF: S/N 3174

E-PROM DATA:

1. PROCESSOR PC BD: 7010-6831-000
   U12002: 3271-6801-140 (V-1.4)*
   U12009: 3271-6802-140 (V-1.4)*

2. PULSE PC BD: 7010-6830-300
   U11005: 3263-6800-240 (V-2.4)*

3. FRONT PANEL PC BD: 7010-6830-200
   U14003: 3271-6803-140 (V-1.4)*

ENHANCEMENTS:

1. AN ON/OFF COMMAND WAS ADDED TO GPIB OPERATION.
2. VERSION NUMBER NOW DISPLAYED DURING INITIALIZATION.
3. ALTITUDE DISPLAY IS BLANK WHEN NO ALTITUDE IS REPORTED.
4. "NO REPLY" IS DISPLAYED ON LOWER HALF OF SCREEN, IF NO REPLY IS FOUND TO A SEQUENCE ITEM.

SYSTEM OPERATION MANUAL: 1002-6801-000
ILLUSTRATED PARTS LIST: 1002-6801-200
SYSTEM DATA - PACKAGE: 1007-6801-000

CORRECTIONS:

1. EXTRA INTERROGATIONS WERE BEING GENERATED IN ACL.
2. S-1403 WILL NOT OPERATE ABOVE SPECIFIED PRF LIMITS.
3. INCREASED ATC MODE PRF LIMIT TO 2400 PRF.
4. PERCENT REPLY NOW REPORTED FOR ATCRBS AND MODE-S IN BOTH ACL AND ACS MODES.
5. ELIMINATED SPURIOUS INTERROGATIONS EMITTED WHEN SWITCHING FUNCTIONS OR CHANGING CW/OFF/NORM SWITCH ON THE ATC-1400A.
6. BURST MODE DISPLAYS DATA FOR SEQ MODE, WHEN PRF IS <400. WITH PRF >400, DF DISPLAY IS NOW BLANK.
7. GPIB RANGE OF P4 IN ACL EXTENDED TO NOW COVER 0.2 TO 3.55 USEC. (UPPER LIMIT WAS 3.2 USEC)
8. IMPROVED GPIB RESPONSE TIME TO: PERCENT REPLY, REPLY DELAY, DOWNLINK REQUESTS.
   (RESPONSE TIME IS DEPENDENT ON PRF RATE + 150 MS DELAY - SEE GPIB PROGRAM TIMING, TABLE 1, S-1403 SERVICE BULLETIN #5)

FM/AM-1200 A/S
FIRMWARE REVISION OUTLINE

FIRMWARE REVISION	EFFECTIVE SERIAL NO.		PAGE
PROCESSOR PC BOARD ASSEMBLY		(8-BIT)	1
1.7	1558	(8-BIT)	2
1.1	1250A/3200S		2
1.2	1250A/3200S		2
1.4	1250A/3200S		2A
1.5	1250A/3200S		2A
1.51	1250A/3200S		2A
PROCESSOR PC BOARD ASSEMBLY		(16-BIT)	3
OPTION-11 ENC/DEC PC BD. ASSY			3A
1.3	OPTION-11		3B
2.0	N/A		4
2.2	1449A/4491S	(16-BIT)	4
2.3	N/A		4
2.4	4762S		4
2.5	1467A/4878S		5
3.0	1697A		5
3.0	5031S		5
FIRMWARE SUFFIX NUMBERS			6
ENHANCED OPT-11 PC BD			6A
ENHANCED OPT-11 PC BD + S.B.-05			6A1
CELLULAR / E-TACS PC BD			6A2
2.3	ENH OPT-11		6B
3.0	ENH OPT-11, OPT-15		6B
3.1	ENH OPT-11, OPT-15		6B
* 3.2	OPT-15		6B

* = CURRENT CHANGES (7/90)

FM/AM-1200 A/S
FIRMWARE REVISION OUTLINE

FIRMWARE REVISION	EFFECTIVE SERIAL NO.	PAGE
4.00	ENH OPT-11, OPT-15, OPT-16	6C
4.01	ENH OPT-11, OPT-15, OPT-16	6C
5.2-XX	6330S	7
5.3-XX	6815S	8
6.0-XX	7847S	9
PROCESSOR PC BOARD ASSY.	(16-BIT)	10
6.1-XX	8617S	11
7.0-XX	10556S	12

* = CURRENT CHANGES (7/90)

VERSION LEVEL AND EFFECTIVITY	ENHANCEMENTS	CORRECTIONS
VERSION 2.2 EFF: S/N 6330(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7730-220	1. ADDS TWO FORMATS: CCIRH (20 MSEC), AND CCIRH4 (40 MSEC). 2. ALL FORMATS NOW ACCEPT 8 DIGITS ON VFD DISPLAY. 3. 5/6 TONE FORMAT NOW ACCEPTS PREAMBLE TONE. 4. DEVIATION SET NOW PROGRAMMABLE TO 7.0 KHZ. 5. "G" CHARACTER AVAILABLE TO DESIGNATE TONE "GROUPS" (OPERATORS MANUAL UPDATE: 1002-5501-007)	1. "ENHANCEMENTS" ACCESSABLE WITH FIRMWARE VER 5.2-XX AND UP. 2. WILL OPERATE IDENTICAL TO ORIGINAL OPT-11 IF INSTALLED IN FM1200, VER 3.0. 3. REFERENCE PAGE 6A FOR E-PROM U7 LOCATION. 4. "ENHANCED" OPTION-11 IS PART OF OPTION-15. 5. ORIGINAL OPTION-11 CANNOT BE UPGRADED.
VERSION 2.3 EFF: S/N 6956(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-230	NONE (OPERATORS MANUAL UPDATE: NONE REQUIRED)	1. DECODING FEATURE WAS INTERMITTENT.
VERSION 3.0 EFF: S/N 7847(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-300	NONE (OPERATORS MANUAL UPDATE: NONE REQUIRED)	1. OCCASIONALLY ON POWER-UP, U22 WOULD NOT LOAD PROGRAM. 2. REFERENCE FM1200S/A S.B.-05 FOR HARDWARE CHANGES.
VERSION 3.1 EFF: S/N 8617(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-310	1. RS-232 COMMANDS ADDED. 2. "A" "B" "C" "D" CHARACTERS NOW VALID DIGITS IN ALL FORMAT SEQUENCES. (OPERATORS MANUAL UPDATE: 1002-5501-008)	1. INCOMPATIBLE WITH SOME LOW COST HAND-HELD AND MOBILE CELLULAR TELEPHONES. NOTE: OPTIONS 11/15 MUST HAVE VER 6.1-XX INSTALLED FOR THIS VERSION.
VERSION 3.2 EFF: S/N N/A E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-311	NONE (OPERATORS MANUAL UPDATE: NONE REQUIRED)	1. CELLULAR VOICE CHANNEL NO LONGER DROPS OUT WHEN TESTING FUJITSU FX CELLULAR TELEPHONE. 2. VER 3.2 IS IDENTICAL TO ENGINEERING PROTO-TYPE VER 3.1.1 FIELDED FOR VERIFICATION. 3. THIS CORRECTION IS INCLUDED IN VER 4.0 AND ABOVE.

VERSION LEVEL AND EFFECTIVITY	ENHANCEMENTS	CORRECTIONS
VERSION 4.00 EFF: S/N 10556S E-PROM DATA: ENC/DEC ASSY, U7: 3271-7703-400	1. ENABLED EUROPEAN TONE TO ENCODE UP TO 8 TONES, INSTEAD OF 5 TONES PER STANDARD SPEC. 2. AUSTRALIAN TWO-TONE PERIOD GAP AFTER FIFTH TONE NOW ENABLED ONLY FOR CCIRH AND CCIRH4. EURO-CODES DO NOT INCORPORATE A TONE GAP AT THIS TIME. 3. ADDS "THRULINE" POWER METER MODULE TO OPT-15/16. (OPERATORS MANUAL UPDATE: 1002-5501-000, REV 06)	1. CHANGED DURATION FROM ONE TONE-GAP TO TWO TONE-GAPS FOR CCIRH AND CCIRH4. (OPT-11) 2. CELLULAR / E-TACS PRINTOUT: A. FROM: 1200S/A, TO: 1200S. B. FROM: TACS, TO: E-TACS. 3. "THRULINE" MODULE P/N: 7005-7740-600. 4. THIS IS NOT A WARRANTY UPDATE - SEE PG. 12.
VERSION 4.01 EFF: S/N 10556S E-PROM DATA: ENC/DEC ASSY, U7: 3271-7703-401	(OPERATORS MANUAL UPDATE: 1002-5501-009)	1. FM1200S WATT METER NOW USED TO MEASURE TYPE 1 PHONE POWER LEVEL 0 (7 WATTS). 2. 75 MS DELAY NOW 300 MS DELAY, AFTER SAT TONE "TURN-OFF" COMMAND. 3. ABOVE CHANGES FOR E-TACS OPTION-16, ONLY.

FM/AM-1200 A/S
FIRMWARE REVISION OUTLINE

FIRMWARE REVISION	EFFECTIVE SERIAL NO.		PAGE
PROCESSOR PC BOARD ASSEMBLY		(8-BIT)	1
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1.1	1250A/3200S		2
1.2	1250A/3200S		2
1.4	1250A/3200S		2A
1.5	1250A/3200S		2A
1.51	1250A/3200S		2A
PROCESSOR PC BOARD ASSEMBLY		(16-BIT)	3
OPTION-11 ENC/DEC PC BD. ASSY			3A
1.3	OPTION-11		3B
2.0	N/A		4
2.2	1449A/4491S	(16-BIT)	4
2.3	N/A		4
2.4	4762S		4
2.5	1467A/4878S		5
3.0	1697A		5
3.0	5031S		5
FIRMWARE SUFFIX NUMBERS			6
ENHANCED OPT-11 PC BD			6A
ENHANCED OPT-11 PC BD + S.B.-05			6A1
CELLULAR / E-TACS PC BD			6A2
2.3	ENH OPT-11		6B
3.0	ENH OPT-11, OPT-15		6B
3.1	ENH OPT-11, OPT-15		6B
* 3.2	OPT-15		6B

* = CURRENT CHANGES (7/90)

FM/AM-1200 A/S
FIRMWARE REVISION OUTLINE

FIRMWARE REVISION	EFFECTIVE SERIAL NO.	PAGE
4.00	ENH OPT-11, OPT-15, OPT-16	6C
4.01	ENH OPT-11, OPT-15, OPT-16	6C
5.2-XX	6330S	7
5.3-XX	6815S	8
6.0-XX	7847S	9
PROCESSOR PC BOARD ASSY.	(16-BIT)	10
6.1-XX	8617S	11
7.0-XX	10556S	12

* = CURRENT CHANGES (7/90)

VERSION LEVEL AND EFFECTIVITY	ENHANCEMENTS	CORRECTIONS
VERSION 2.2 EFF: S/N 6330(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7730-220	1. ADDS TWO FORMATS: CCIRH (20 MSEC), AND CCIRH4 (40 MSEC). 2. ALL FORMATS NOW ACCEPT 8 DIGITS ON VFD DISPLAY. 3. 5/6 TONE FORMAT NOW ACCEPTS PREAMBLE TONE. 4. DEVIATION SET NOW PROGRAMMABLE TO 7.0 KHZ. 5. "G" CHARACTER AVAILABLE TO DESIGNATE TONE "GROUPS" (OPERATORS MANUAL UPDATE: 1002-5501-007)	1. "ENHANCEMENTS" ACCESSABLE WITH FIRMWARE VER 5.2-XX AND UP. 2. WILL OPERATE IDENTICAL TO ORIGINAL OPT-11 IF INSTALLED IN FM1200, VER 3.0. 3. REFERENCE PAGE 6A FOR E-PROM U7 LOCATION. 4. "ENHANCED" OPTION-11 IS PART OF OPTION-15. 5. ORIGINAL OPTION-11 CANNOT BE UPGRADED.
VERSION 2.3 EFF: S/N 6956(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-230	NONE (OPERATORS MANUAL UPDATE: NONE REQUIRED)	1. DECODING FEATURE WAS INTERMITTENT.
VERSION 3.0 EFF: S/N 7847(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-300	NONE (OPERATORS MANUAL UPDATE: NONE REQUIRED)	1. OCCASIONALLY ON POWER-UP, U22 WOULD NOT LOAD PROGRAM. 2. REFERENCE FM1200S/A S.B.-05 FOR HARDWARE CHANGES.
VERSION 3.1 EFF: S/N 8617(S) E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-310	1. RS-232 COMMANDS ADDED. 2. "A" "B" "C" "D" CHARACTERS NOW VALID DIGITS IN ALL FORMAT SEQUENCES. (OPERATORS MANUAL UPDATE: 1002-5501-008)	1. INCOMPATIBLE WITH SOME LOW COST HAND-HELD AND MOBILE CELLULAR TELEPHONES. NOTE: OPTIONS 11/15 MUST HAVE VER 6.1-XX INSTALLED FOR THIS VERSION.
VERSION 3.2 EFF: S/N N/A E-PROM DATA ENC/DEC ASSY, U7: P/N 3271-7703-311	NONE (OPERATORS MANUAL UPDATE: NONE REQUIRED)	1. CELLULAR VOICE CHANNEL NO LONGER DROPS OUT WHEN TESTING FUJITSU FX CELLULAR TELEPHONE. 2. VER 3.2 IS IDENTICAL TO ENGINEERING PROTO-TYPE VER 3.1.1 FIELDED FOR VERIFICATION. 3. THIS CORRECTION IS INCLUDED IN VER 4.0 AND ABOVE.

VERSION LEVEL AND EFFECTIVITY	ENHANCEMENTS	CORRECTIONS
VERSION 4.00 EFF: S/N 10556S E-PROM DATA: ENC/DEC ASSY, U7: 3271-7703-400	1. ENABLED EUROPEAN TONE TO ENCODE UP TO 8 TONES, INSTEAD OF 5 TONES PER STANDARD SPEC. 2. AUSTRALIAN TWO-TONE PERIOD GAP AFTER FIFTH TONE NOW ENABLED ONLY FOR CCIRH AND CCIRH4. EURO-CODES DO NOT INCORPORATE A TONE GAP AT THIS TIME. 3. ADDS "THRULINE" POWER METER MODULE TO OPT-15/16. (OPERATORS MANUAL UPDATE: 1002-5501-000, REV 06)	1. CHANGED DURATION FROM ONE TONE-GAP TO TWO TONE-GAPS FOR CCIRH AND CCIRH4. (OPT-11) 2. CELLULAR / E-TACS PRINTOUT: A. FROM: 1200S/A, TO: 1200S. B. FROM: TACS, TO: E-TACS. 3. "THRULINE" MODULE P/N: 7005-7740-600. 4. THIS IS NOT A WARRANTY UPDATE - SEE PG. 12.
VERSION 4.01 EFF: S/N 10556S E-PROM DATA: ENC/DEC ASSY, U7: 3271-7703-401	(OPERATORS MANUAL UPDATE: 1002-5501-009)	1. FM1200S WATT METER NOW USED TO MEASURE TYPE 1 PHONE POWER LEVEL 0 (7 WATTS). 2. 75 MS DELAY NOW 300 MS DELAY, AFTER SAT TONE "TURN-OFF" COMMAND. 3. ABOVE CHANGES FOR E-TACS OPTION-16, ONLY.