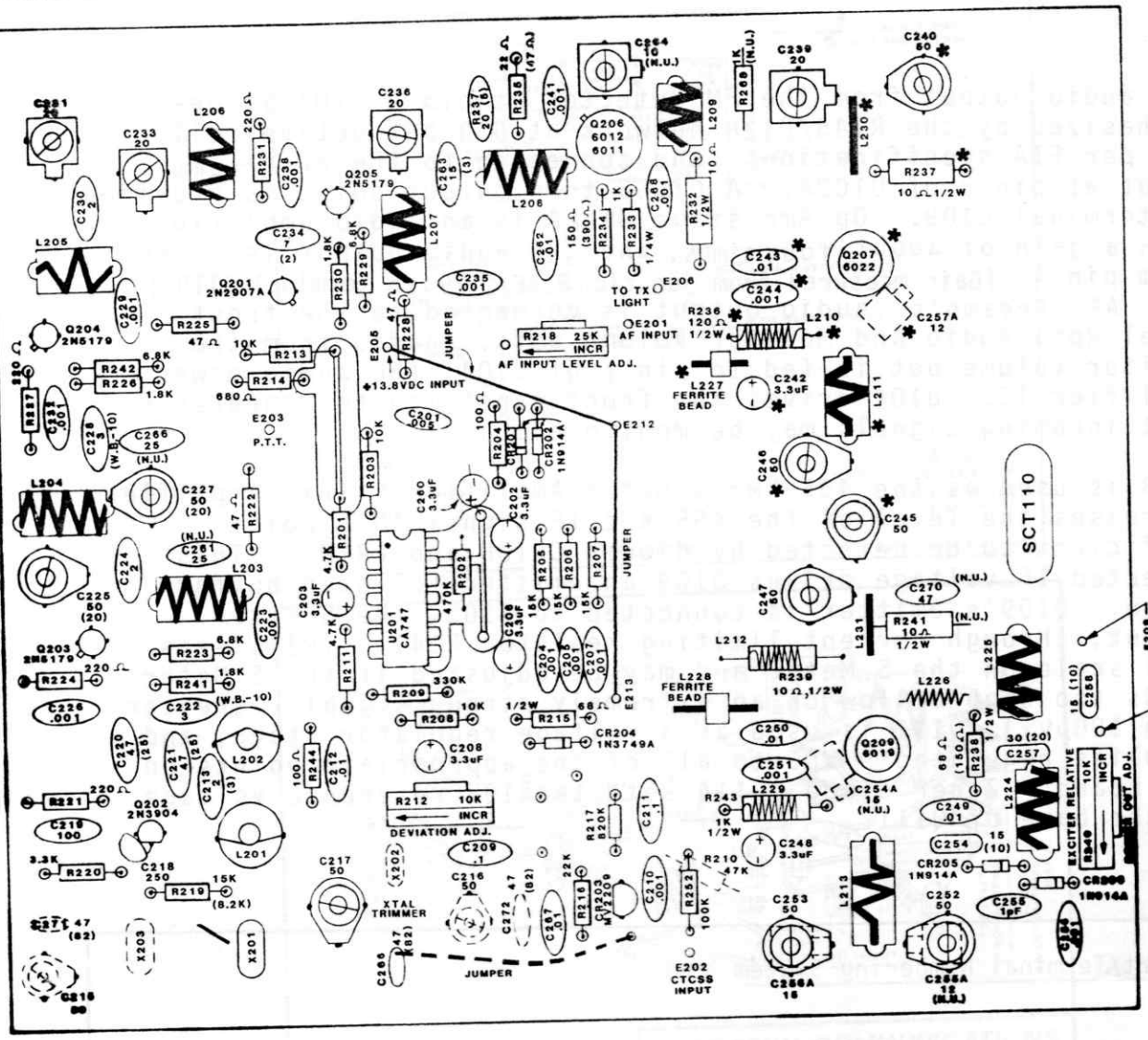
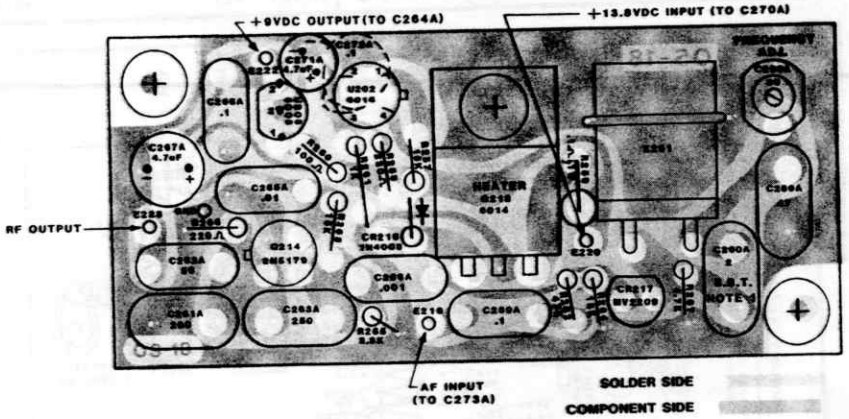


NOTES:
1)VALUES IN ( ) ARE FOR 216-250MHz. (N.U.) NOT USED FOR 216-250MHz.
2)NOT ALL PARTS SHOWN ARE USED ON ALL VERSIONS OF THE SCT110.
3) ● DENOTES EXTRA PARTS USED FOR 216-250MHz AND NOT USED FOR 136-174MHz.

SPECTRUM COMMUNICATIONS		
SCALE	APPROVED BY	DRAWN BY R.L.A.
DATE 2-20-80		REVISED 6-13-84
SCT110 TX BD. COMPONENT LAYOUT (SCR1000)		DRAWING NUMBER 3200111



NOTE:
1)THIS CAP IS SELECTED TO CENTER CRYSTAL FREQUENCY.(0-10pF TYP.)

136-174MHz & 216-250MHz

SPECTRUM COMMUNICATIONS		
SCALE	APPROVED BY 6/7/84	DRAWN BY R.L.A.
DATE 4-7-80		REVISED 5-31-84
CRYSTAL OSCILLATOR OVEN MODULE		DRAWING NUMBER 2200118

FIGURE 7

6.2 TRANSMITTER

Initial FM signal generation is accomplished at Q202 and its supporting circuitry. This stage is a modified Clapp oscillator with the 18 MHz crystal operating on the inductive slope of its parallel resonance curve. The collector circuit of Q202 is resonated at the second harmonic of the crystal frequency, (third harmonic on 220 MHz versions), by a double-tuned filter, and is applied to the base of Q203, a frequency doubler. FM modulation is affected by "modulating" the crystal load capacitance with varactor diode CR203. A steady-state D.C. bias for CR203 is provided by R217, and the modulating audio signal is superimposed on this voltage through C209.

Modulating audio for CR203 is pre-emphasized by R203, and C201, and is applied to IC201A where it is amplified by a factor of 10. The output of IC201A is applied to "back-to-back" diodes CR201 and CR202 which cause the audio signal to be limited to a maximum value of about 1.4 Vp-p. The limited audio signal is next applied to a 3 section RC lowpass filter which removes most of the high order harmonic distortion produced by the limiting process. The output of the lowpass filter is fed to IC201B for further amplification, and is finally connected to the varactor modulator through Deviation Pot R212.

The RF drive to Q203, now at 37 MHz (55 MHz in 220 MHz versions), is doubled in frequency and is filtered by another double tuned circuit before being applied to the base of Q204. Q204 is another frequency doubler, and the 75 MHz drive at its base (110 MHz in 220 MHz versions), is multiplied in the collector circuit to 150 MHz (220 MHz), the final output frequency. The signal is again filtered in a double-tuned circuit, and is fed to the base of pre-driver Q205. The signal is further amplified by Q206, and is applied as drive to the Class "C" amplifier chain consisting of Q207 and Q208. (In 136-174MHz repeater applications, the output from Q206 is applied directly to Q208, and Q207 is eliminated. Power output from Q208, about 8-10 watts in 136-174MHz units, (10-12 watts in 220MHz versions) is routed to the RF output terminal on the board. A sample of the RF output from Q208 is picked off and rectified by CR205 and CR206 to drive the Relative Output meter.

For high stability applications, (FCC Type Accepted unit, etc.), the OS-18 Crystal Oscillator/Oven is used. Q214 is the oscillator transistor which is operated in the Clapp configuration in the 17-22 MHz range. U202 is the precision Temperature Controller IC which maintains the oven temperature at +80°±2°C. Q213 is the power transistor employed as an effective heating element for the oven. The Temperature Controller is a proportional type which smoothly controls the temperature of the crystal and all of the oscillator components. This results in extremely good frequency stability, even over very wide temperature excursions, far superior to that of typical TCXOs! The oscillator's output drives the base of multiplier transistor Q202. See schematic diagram - Figure 8.

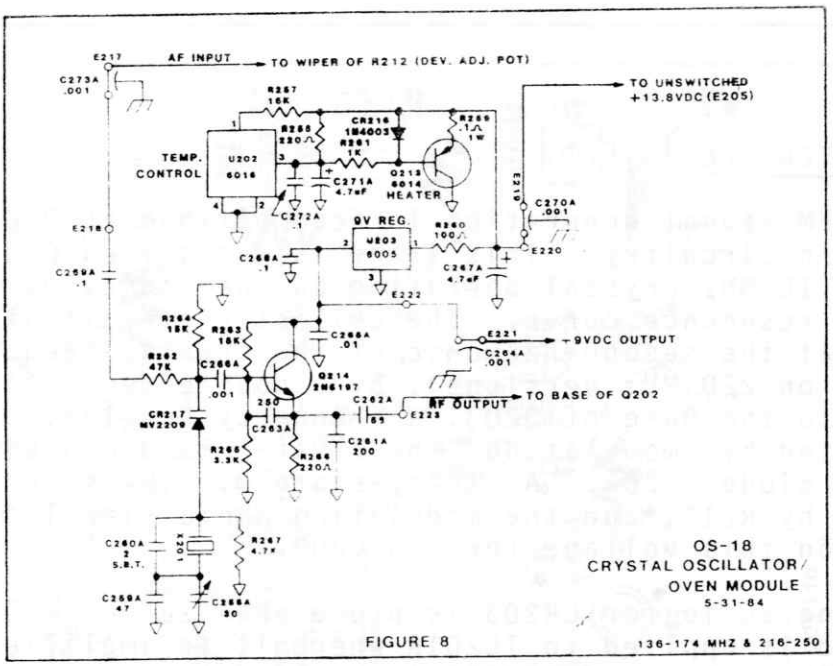
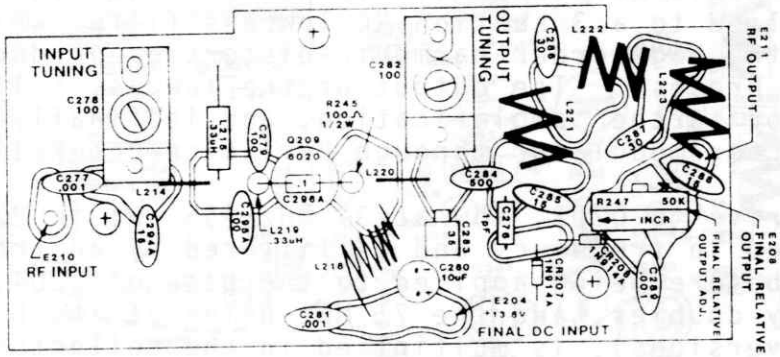


FIGURE 8

136-174 MHZ & 216-250



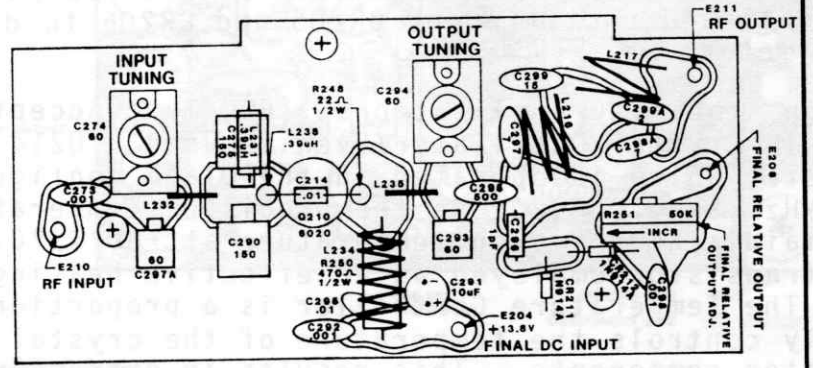
SPECTRUM COMMUNICATIONS

SCALE		APPROVED BY	DRAWN BY R.L.A.
DATE 5-24-84		6/1/84 5/29/84	REVISED

BA-30 AMPLIFIER BOARD
COMPONENT LAYOUT
DRAWING NUMBER 1200136

FIGURE 9A

136-174MHz



SPECTRUM COMMUNICATIONS

SCALE		APPROVED BY	DRAWN BY R.L.A.
DATE 5-23-84		6/7/84 5/29/84	REVISED

BA-20 AMPLIFIER BOARD
COMPONENT LAYOUT
DRAWING NUMBER 1200135

FIGURE 9B

216-250MHz

The 13.8 VDC input is applied directly to Class "C" stages Q207 and Q208, and also to audio stage IC201. Oscillator stage Q202 is run continuously from a 9 volt zener diode regulator for maximum stability. Grounding the PTT input to Q201 causes Q201 to turn on, applying +13.5 volts to both frequency doubler stages and both pre-driver stages.

The RF output of exciter board is next applied to the final amplifier board. The final amplifier is Q209 (or Q210), an emitter ballasted RF power transistor. The power amplifier is designed with sufficient heat-sinking to provide a nominal output of 30 Watts in continuous service when operated into a proper 50 ohm load. The power transistor is capable of withstanding open and shorted load conditions for short periods of time, but this should be avoided, since certain VSWR conditions can cause excessive heat build-up in the amplifier and possibly damage the device.

The output of the amplifier is passed through a 3 section (2 section on 220 MHz) lowpass filter which greatly attenuates all harmonics. A diode rectifier provides a relative indication of peak output voltage which is sampled just ahead of the lowpass filter. R247 is set for a relative final output reading of 6-8 on the meter for approximately 30 Watts out to a 50 ohm load.

6.3 CONTROL/TIMER/COR BOARD (CTC100B)

Referring to the schematic, the COR trigger output from the receiver is connected to terminal E323 on the COR board. This trigger voltage is in a "high" state with no received signal (squelch closed); and it switches "low" with received signal (squelch open). The voltage is dropped to a lower level by resistive voltage divider R313 and R314, and then applied to one input (pin 6) of NOR gate U302D. The remaining input of U302D is driven from the output of U303A, a flip-flop which is toggled by the front panel "COR SIMULATE" indicator lamp driver. The output of U302D, then, is a logic "high" in the presence of either a simulated or an actual signal acquisition, and is used to drive Q303, the "INCOMING SIGNAL" indicator lamp driver. This logic level is switched by the front panel "COR DISABLE" switch and is used to trigger the "HANG" timer which consists of Q301, and NOR gates U301A and U301B.

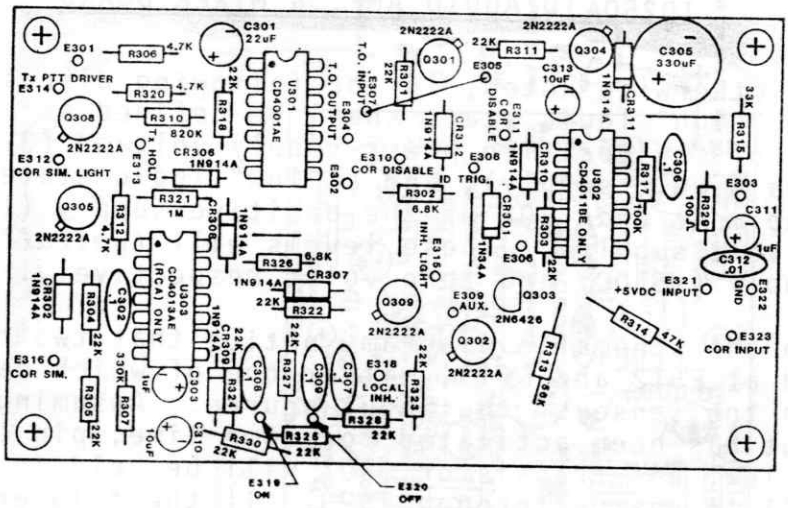
The HANG timer works in the following manner: A "COR" activation causes pin 9 of U301B to go "high" which in turn causes the U301A/U301B flip-flop to be set. Simultaneously, transistor Q301 is turned on, causing the 20uF capacitor to rapidly discharge. At this point, pins 3 and 10 of U301 are at logic levels "one" and "zero" respectively, and remain in this state as long as the COR is activated. Upon deactivation of the COR, pin 9 of U301B goes "low", and transistor Q301 turns off, allowing the 20uF capacitor to charge through R602, the front panel "HANG TIME" pot.

When the 20uF capacitor has charged to the threshold point of U301A, the U301A-U301B flip-flop is reset and returns to the standby mode.

The "TIME-OUT" timer operates in the following manner: Upon activation of the COR, and for the duration of COR activation, pin 3 of U301 will be high, and pin 10 of U301, as well as pin 11 of U301, will be low. The low condition on pins 10 and 11 of U301 will cause transistor Q304 to be in the off state, and the high condition on pin 3 will cause the 330 uF capacitor to charge through the front panel "TIME-OUT" pot. When the voltage on the 330 uF capacitor reaches the threshold of U302A, pin 1 of U302B will go "low", triggering the U302B-U302C flip-flop. At this point the timer is in the "timed-out" state with pins 3 and 10 of U302 at logic "one" and "zero" respectively. The timer remains in this state until a negative transition appears at board terminal #5, at which time the U302B-U302C flip-flop will be reset. Depending on which jumper wire configuration is selected (term #E305 and E304, or term #E305 and E307) time-out reset will occur either upon COR deactivation (removal of RCVR signal) or upon "HANG" timer reset (transmitter drop).

The normally low output from the time-out timer and the active low output from the hang timer are summed in COR gate U302D, which turns on the transmitter PTT driver, Q308. Also summed into U301D is the output of the reset-inhibit flip-flop, U303B. Momentary activation of the inhibit lamp driver, Q309. A pair of inputs are provided for remote inhibit and reset through terminals E320 and E319 respectively.

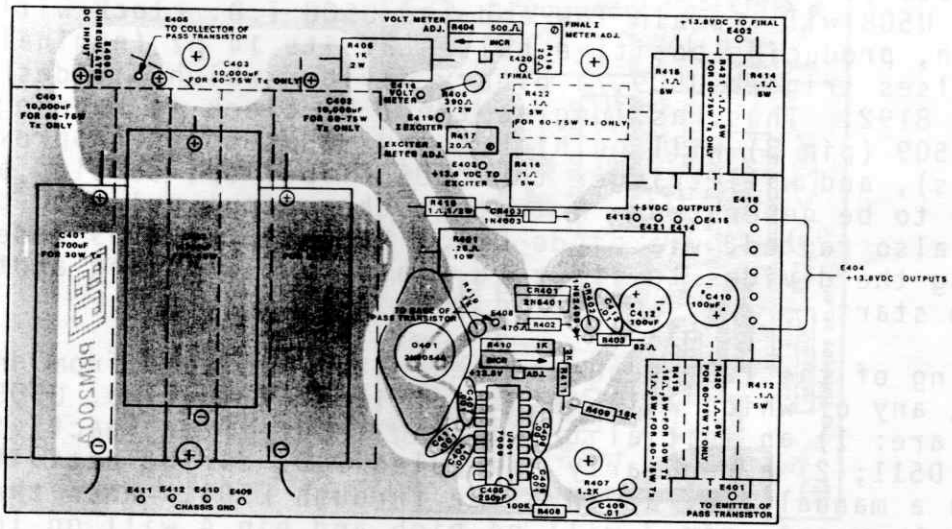
A positive going pulse or DC level shift of +5V amplitude on pin E320 will inhibit the transmitter, while a similar pulse on pin E319 will reset the unit to normal operation.



SOLDER SIDE

FIGURE 10

SPECTRUM COMMUNICATIONS		
SCALE	APPROVED BY	DRAWN BY R.L.A.
DATE 7-5-83		REVISED 5-25-84
COR/TIMER/CONTROL BOARD		
CTC100B		DRAWING NUMBER 1300104B



SOLDER SIDE

FIGURE 11

SPECTRUM COMMUNICATIONS		
SCALE:	APPROVED BY:	DRAWN BY R.L.A.
DATE: 5-11-84		REVISED
PRM200A POWER SUPPLY COMPONENT		
LAYOUT		DRAWING NUMBER 3200144

ID250A ID/AUDIO AMP. & MIXER BOARD

NOTE: Unless otherwise noted, in the following discussion any reference to a "high" logic state shall be defined as a voltage of *at least* 70% of the positive power supply voltage (3.5 volts in the case of a 5 volt supply), and a "low" logic state shall be a voltage of *no more than* 20% of the positive supply (1 volt in the case of a 5 volt supply). These levels will *typically* be full positive supply (+5VDC) and zero volts respectively.

Referring to the schematic diagram, notice that two trigger inputs are provided at E512 and E513, either one of which can be used, depending on the sense of the input source. Assuming that neither trigger input has been activated for some time, pin 10 of U504 will remain low, and transistor Q503 will be held in the off state, allowing C511 to charge through R529. If the trigger inputs remain inactive long enough (approximately 1½ minutes), C511 will charge up to the threshold point of the U508 flip-flop, causing pin 4 of U508 to go high and pin 3 of U508 to go low. The high state on pin 4 causes the I.D. timer clock to stop (via the high state on pin 8 of U508), and simultaneously resets the I.D. clock counter, U509, to its zero state. The unit is now in the standby condition, and will be activated immediately upon the next trigger input.

When a trigger signal arrives, it will cause pin 10 of U504 to go high, which in turn, causes the U508 flip-flop to be set, and also causes Q503 to keep C511 discharged as long as there is input activity at intervals of less than 1½ minutes. As soon as the U508 flip-flop is set, the high level on pin 3 is converted by C502 and R513 into a short positive going spike which passes through D511 and sets the trigger flip-flop, U505, causing an I.D. to be generated immediately. (Details of the I.D. generation sequence will follow later). As long as the activity timer detects input activity, pin 4 of U508 will remain low and the U508 I.D. clock will be allowed to run, producing positive pulses at its 14 Hz (nominal) rate. These pulses trigger U509, a binary divider which divides the 14 Hz clock by 8192. Thus, as long as the I.D. clock is running, the output of U509 (pin 3) will go high every 585 seconds (approximately 10minutes), and will trigger the U505 flip-flop, causing an I.D. sequence to be generated. Note that the output pulse on pin 3 of U509 is also routed, via diode D513, back to the U509 reset input, resetting the divider to its zero state, and allowing another timing cycle to start.

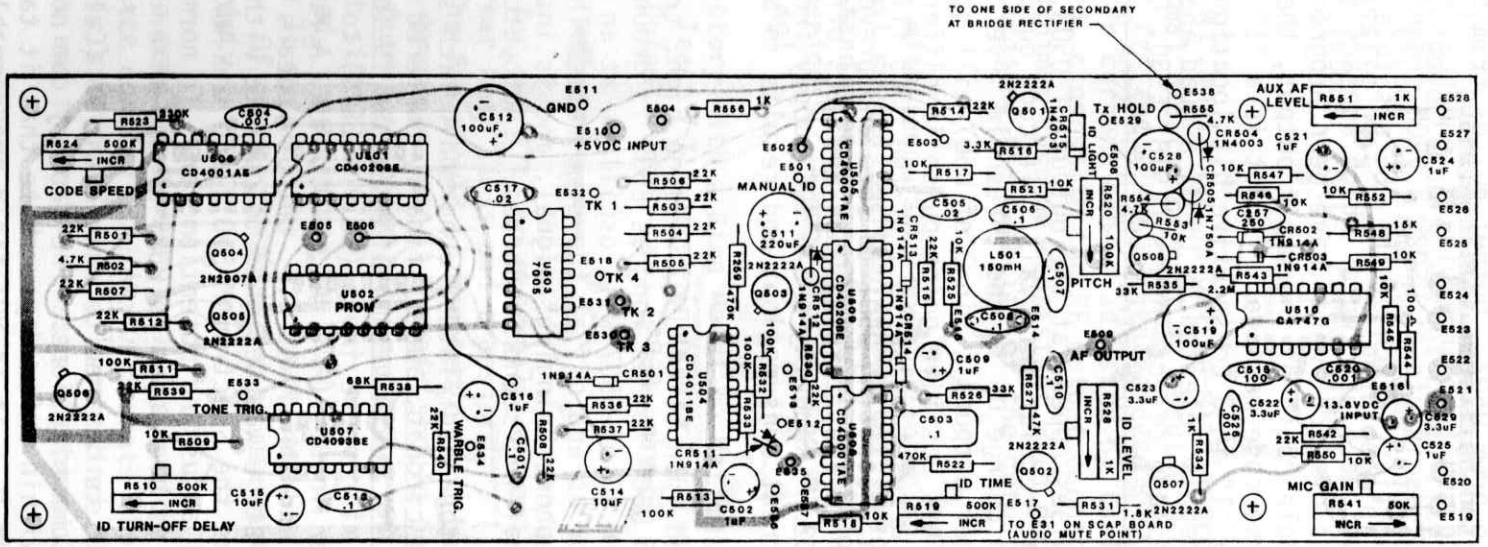
Triggering of the I.D. sequence generator can come from one of 3 sources, any of which will set the trigger flip-flop, U505. These sources are: 1) an initial triggering input after inactivity, through D511; 2) a regularly scheduled I.D. during activity, through D512; 3) a manual I.D. at any time through E501. When the U505 flip-flop has been set, pin 3 will go high and pin 4 will go low. The high on pin 3 causes Q501 to turn on (assuming that E502 and E503 are jumpered), clamping the transmitter hold output (E529) to ground for the duration of the I.D. cycle.

NOTES:

1)U502-7017 or 7031.

2)E505 WILL TURN-OFF PROM AFTER 128 BITS WHEN CONNECTED TO E507.

3)E506 WILL TURN-OFF PROM AFTER 256 BITS WHEN CONNECTED TO E507.



SOLDER SIDE

COMPONENT SIDE

FIGURE 12

SPECTRUM COMMUNICATIONS		
SCALE:	APPROVED BY	DRAWN BY R.L.A.
DATE: 2-20-84	6/18/84	REVISED
ID250A COMPONENT LAYOUT		
ID & AUDIO BOARD		DRAWING NUMBER 3200143

The low-on pin 4 of U505 causes binary counter, U501, to be released from its reset state (a high on the reset input keeps the counter from toggling). When pin 4 of U505 is low, pin 3 will be high, turning on Q504 & Q505, and enabling the 5 VDC supply to prom U502. Output pulses from the code speed oscillator, U506, cause U501 to count up in a binary sequence, and the binary outputs are applied to the address inputs of U502, a PROM organized in a 256 bit long by 4 bit wide configuration. Each of the 256 possible binary outputs from U501 corresponds to a unique 4 bit "word" which appears at pins 9, 10, 11, & 12 of U502. The contents of each "word" have been programmed at Spec Comm so that, looking at any single "bit" of the 4 bit output, the sequence of 1's and 0's represents the morse code message. (A dot is a "1" in 1 bit location, while a dash consists of a "1" in 3 consecutive bit locations.) The particular 1 bit data channel desired is selected by U503, a quad analog switch. A high on anyone of the 4 message select inputs (E518, E530, E531, E532) will cause one of the 4 outputs of U502 to control the U505 tone oscillator.

As long as code pulses appear at the output of U503, transistor Q506 will keep discharging C515 at regular intervals. If code output from U503 ceases long enough for C515 to charge up to the threshold level of U507 (a quad NAND gate with schmitt trigger outputs), pin 3 of U507 will go low, and pin 4 of U507 will snap high. This positive going pulse is differentiated by C513 and R536, and is applied as a reset pulse to 1 of the U505 flip-flop. When U505 is reset, pin 4 will go high, resetting U501 to zero and preventing any further counting. Pin 3 of U505 will go low, turning Q504 and Q505 off, thus removing the 5 VDC supply to PROM U502. (Removing the 5 VDC supply from U502 during standby saves about 80 mA of current consumption, and results in a standby current draw of about 5 mA.)

If E533 is grounded, pin 11 of U507 will go high, triggering the U505 tone oscillator through U506 for as long as E533 is grounded. If E534 is raised to a "high" level, pin 10 of U507 will oscillate at an approximate 20 Hz rate keying the tone oscillator on and off at the same rate. This sound is intended to approximate a telephone "ringing" signal, and is intended for applications where a distinctive signalling sound is needed. (Autopatch, etc.)

The output of the tone oscillator, a harmonic rich square wave, is filtered by the L501/C506-508 tank circuit, and is finally buffered by emitter follower stage Q502. A 4 input dual Op Amp audio preamplifier/mixer is incorporated onto the ID250 board. The local microphone input (E519 & E520) to this stage is amplified by U501A. The 3 other inputs (RPT. AF, I.D., AUX. A.F.) are resistively summed with the U501A output, and the mixed A.F. output appears at E521 as composite repeater audio. The IC501 stage was designed to operate with a medium impedance ceramic microphone (such as the Spectrum M-510), and the AUXILIARY A.F. INPUT has been provided with a level adjusting potentiometer. In normal use the audio output from E509 of the ID'er is connected to E525 of the mixer.

I.D. MEMORY: If it is desired to *change the ID* (Call Letters) in the memory, contact Spectrum Communications. The factory can normally program and ship a new PROM memory chip within a few days. Note that it takes special factory equipment to program the PROM IC - it is *NOT* field programmable. (Simply take the PROM out of its socket, and plug in the new PROM.)

6.5 75 WATT TRANSMITTER OPTION

6.5.1 INTRODUCTION

The 75 Wt. SCR1000 is a special version of the SCR1000 Repeater. It includes a higher power transmitter exciter board, a final amplifier board which uses 2 RF output transistors; increased power supply current capability with a larger power transformer and electrolytic filter cap, and two "super rugged" 200W/30A pass transistors in parallel. Massive heat sinks are provided for the pass transistors and the final amplifier transistors. (Note: rated output is 65W nom. 216-230MHz.)

6.5.2 OPERATION

In normal operation, the 75 Wt.amplifier is driven with approx. 10 watts of power from the exciter board. Normal exciter current is about 2.0-2.5A. Normal final current is 7.5-9.0A. *Do not let the final current exceed 9.5A!* (For best long-term reliability.) Final Amplifier current can be adjusted by tuning the Output Tuning Cap C283A, on the final board, closest to the RF Output connector. Always tune for best efficiency! i.e. Minimum current consistant with good power output. (Typically achieved when *increasing* the capacity of the output tuning cap -CW- towards max capacity.)

The amplifier is designed to withstand VSWRs up to 3:1 for as much as 5 minutes. Although the amp uses the most rugged "emitter ballasted" transistors available, it was not designed to withstand open or shorted load conditions, (although it may do so for very short periods). A good 50 ohm load must always be connected the output before transmitting!

The unit was tuned at the factory with a Bird Model 43 Wattmeter into the 50 ohm load. If you do not read at least 70W output into your system, a slight adjustment of the above mentioned Output Tuning cap, C283A, may be required.

6.5.3 COOLING - IMPORTANT!

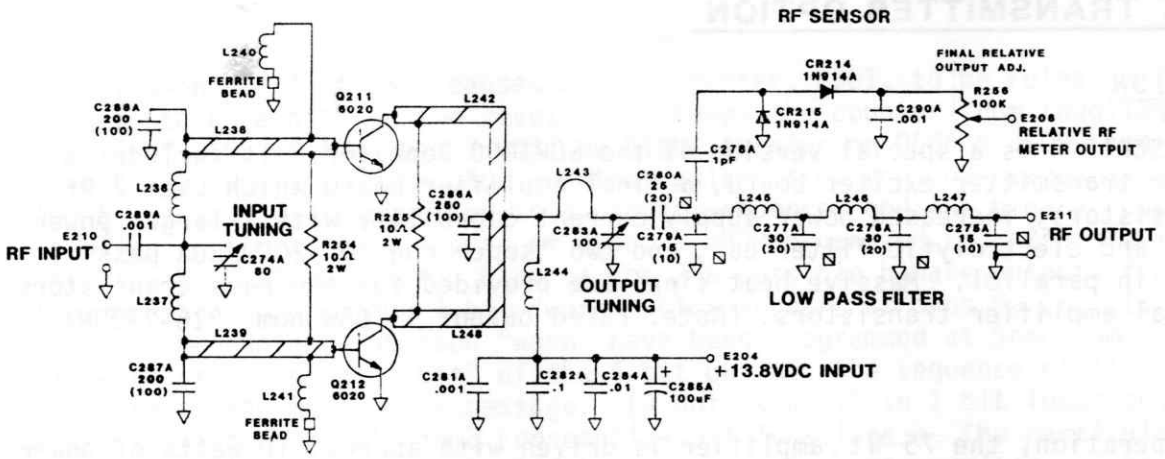
This amplifier was designed for use with an external (optional) "Muffin" fan which blows cooling air over the rear heat sinks and transformer. (120 c.f.m. *minimum* fan rating must be used.) The fan should be mounted on the back door of the rack or cabinet used, or on metal brackets, etc. The air should be carefully directed so the 2 *heat sinks and the transformer are all in the air stream.* (Fan should be about 8-12" behind the 2 heat sinks.)
Although it is not recommended, the unit may be used without a fan for short duty cycle operation, (i.e. up to 15 minutes max. transmit time, with at least a 30 minute cooling down period.) Of course, *with* the fan, maximum transmit time is unlimited. (100% continuous duty.)

In any case, the unit must be mounted so that *both* the bottom of the chassis, and the rear sinks are *open to free cooling air!* Never operate the unit for more than a few minutes with the chassis sitting flat on a bench since this blocks the cooling air to the heat sinks and the under-chassis components!

6.5.4 METERING, ETC.

Note that for the 75 Wt. transmitter, both front panel current meters read *2 times normal indication;* i.e. the exciter current is 3.0A full scale, (2x the 1.5A scale; and the final current is read on the *15A scale*).

Normal B+ to the final, as measured at the feed-through cap on the transmitter housing is 13.0 to 13.8VDC max. while transmitting.

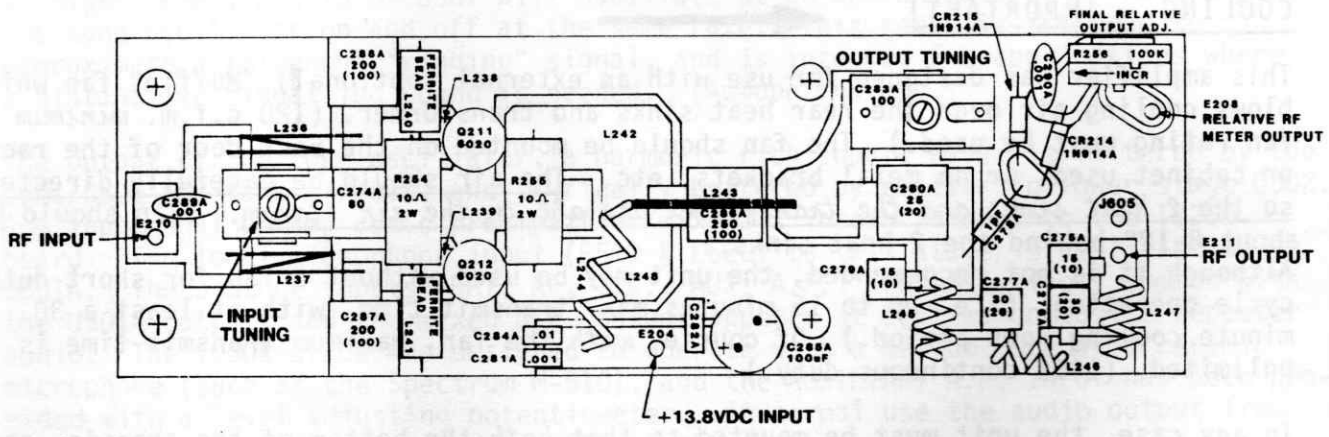


NOTES:

1) ⧄ INDICATES CHIP CAPS.
2) ( )DENOTES VALUE CHANGES FOR 216-230MHz.
3)POWER OUTPUT IS 60W MIN. FOR 216-230MHz.

SPECTRUM COMMUNICATIONS		
SCALE:	APPROVED BY:	DRAWN BY R.L.A.
DATE: 7-22-80		REVISED 5-30-84
BA-75RPT AMP. SCHEMATIC		
136-174 & 216-250MHz		DRAWING NUMBER 2200119

FIGURE 13



NOTES:

1) ( )DENOTES VALUE CHANGES FOR 216-230MHz.
2)POWER OUTPUT IS 60W MIN. FOR 216-230MHz.

SPECTRUM COMMUNICATIONS		
SCALE:	APPROVED BY:	DRAWN BY R.L.A.
DATE: 7-21-80		REVISED 5-30-84
BA-75RPT AMP. LAYOUT		
136-174 & 216-250MHz		DRAWING NUMBER 2200117

FIGURE 14

6.5.5 LOAD VSWR

Important: For maximum operating life and best reliability, *be sure that the load VSWR does* not exceed 1.5:1! (When a duplexer is used, this is the VSWR *looking into the duplexer's TX Input.*) Also, *do not tune* the duplexer while transmitting at the 75W level since *extremely high* VSWR loads can be presented to the amp when the duplexer is de-tuned. A high VSWR load could possibly cause damage to the output circuitry if the transmitter is keyed for a prolonged period of time.

6.5.6 AC POWER TRANSFORMER PRIMARY TAPS

The transformer in the SCR1000 is normally wired with the primary tap at the 115VAC point. This tap is the optimum point for operation over an AC line voltage range of about 110-120VAC. If the actual line voltage (while transmitting) is above or below these limits, the primary tap wire should be changed accordingly. For example, if the line voltage is in the area of 108VAC, change the tap from the 115 to the 105VAC tap. Likewise, if the line voltage is greater than 120VAC, change the tap to the 125VAC lug.

75 Wt. Amp.
LIMITED WARRANTY: 60 Days parts and labor on the BA-75RPT Board itself. 180 days parts and labor on the rest of the SCR1000 Repeater. The *Warranty is voided if a cooling fan is not used.*

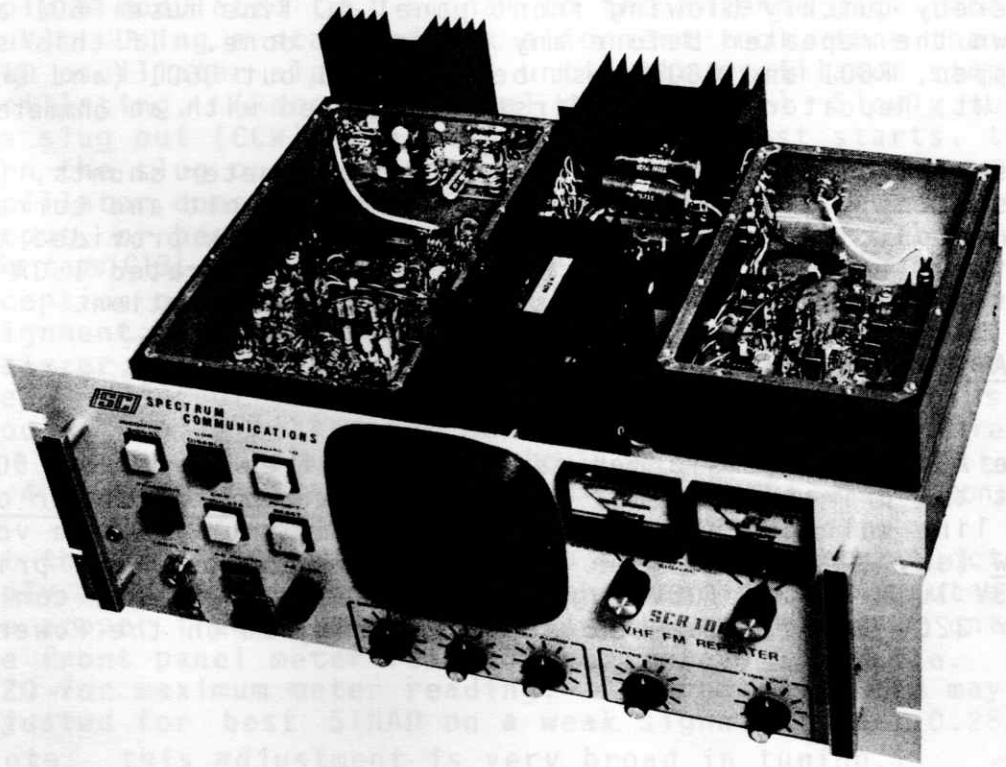


FIGURE 15 - 75 WATT REPEATER/BASE STATION
NOTE LARGER HEATSINKS, TRANSFORMER, AND POWER AMP BOARD

6.6 POWER SUPPLY

6.6.1 The standard power supply consists of a heavy-duty 12A power transformer, 35A bridge rectifier, 30A/200W pass transistor(s) mounted on a massive heat sink, and an IC voltage regulator/metering board. The AC line input is fused, and protected from line spikes and transients by a high-capacity MOV (Metal Oxide Varistor) transient suppressor. The supply is very conservatively designed - normal current draw is only 5.5A (10.5A for a 75W unit). C401, 2 & 3 are used to filter the rectified AC. U401 is a feedback voltage regulator which drives the Darlington pass transistor configuration made up of Q601 and Q401. These 2 power transistors provide a very high overall current gain of over 1000. The regulator also includes a "foldback current limiting" feature which automatically and instantly "folds-back" the supply's output to a very low voltage and current if the output is shorted - thereby protecting the supply. This circuit provides excellent regulation and filtering - ripple is less than 10mVp-p at an 8A load.

6.6.2 An overvoltage "crowbar" shutdown circuit is used to shutdown the power supply in the unlikely event that the pass transistor should short out. If Q601 does short, zener diode CR402 will conduct, thereby turning on SCR CR401. When CR401 conducts, it will draw a very large current through R401 for a few hundred milliseconds, thereby quickly blowing front panel AC line fuse F601 and shutting down the repeater before any damage is done. If this should happen, F601 and Q601 must be replaced, but Q601 (and Q602 for the 75 Wt. Repeater) should first be checked with an ohmmeter for shorts.

6.6.3 Also included on this board are various meter shunts, (wire wound resistors), and calibration pots for the volt and current meter functions. A separate fixed 5V regulator is provided to supply this voltage to the logic circuitry. It is rated 1.3A and has built-in current limiting/short-circuit protection.

6.6.4 CHANGING POWER TRANSFORMER TAPS

The AC Power Transformer is normally wired for 115V, 50-60Hz input, but the primary taps may be easily rewired for higher or lower AC line voltage input. For Example: if your AC line voltage is low (say 104-110V), then move the wires on the T601 primary from the 115V lugs to the 105V lugs. Likewise, the primary can be wired for 220V input. See the schematic diagram on the Power Supply.