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REVISION 1
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Granger
Associates

INSTRUCTION MANUAL

MODEL 6710
POINT TO MULTIPOINT UHF RADIO

SCANCOM
1200M/9600M MASTER
AND
1200R/9600R REMOTE
SHELF MOUNTED

001-9820
RECEIVER

GRANGER ASSOCIATES

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RECEIVER MODULE

PART NUMBER 001-9820-XX*

(* where XX = the Option Suffix number)

REFERENCE

Block Diagram Figure 1
Schematic Diagram 071-8091
Top Assembly 001-9820
PCB Assembly/Parts List 065-2625

1. FUNCTION

1.01 The Receiver module operates continuously in both the Hot-Standby and Non-Standby Radios.

1.02 If provided in an HST redundant configuration, the VF and Squelch outputs of both Receiver modules are fed to the Combiner module.

1.03 The L.O. frequency for both the Receiver and Transmitter modules is provided by the Receiver, and is used to upconvert the Transmitter to its output RF frequency, while it downconverts the received RF input (from the Diplexer) to the Receiver I.F. frequency. This 10.7 MHz I.F. is then demodulated for output to the Combiner or Interface modules.

OPTIONS

-98 Scancom 1200/9600 Master
-99 Scancom 1200/9600 Remote

Crystals are added from kit 091-7997 to select frequency. Earlier receiver models had their frequencies called out as an option. This option is identical to the option now selected from the crystal kit and fitted to one of the current options.

INPUTS

J4 RX IN
J1-3 +13.6 Vdc
J1-1 GND

OUTPUTS

J2 LO OUT
J3 LO FREQ TEST (90 - 100 MHz)
J1-8 LOW LO PWR (ALM)
J1-6 AUDIO OUT
J1-9 SQUELCH OUT

TEST POINTS

RX LEVEL (Front Panel)

ADJUSTMENTS

C55 FACTORY SEL (FOR LO FREQ)
C56 LO FREQ ADJ
C73 Q9 (X2 MULT OUTPUT ADJ)
C77 Q10 (X10 MULT OUTPUT ADJ)
R95 SQUELCH ADJ (Front Panel)
R86 VF OUTPUT LEVEL ADJ

STRAPS

Before Q3 - After FL2 (Remove for testing only)

Adjacent R132 - Audio bypass of U9 in Hot-Standby Terminals (not fitted on current production NST and HST models).

SWITCHES/INDICATORS

DS2 RX SIGNAL (GRN LED)

2. CIRCUIT DESCRIPTION
RECEIVER MODULE

2.01 The received RF signal from the Diplexer is input to J4 (RX IN) on the front of the Receiver module.

2.02 The signal is amplified 26 dB by RF amplifier Q1 and Q2, and filtered by bandpass filter FL1 to reject image frequencies.

2.03 It is then downconverted to the first intermediate frequency (I.F.) of 10.7 MHz by mixing it with the reference L.O. signal in mixer MXR-1.

2.04 The 10.7 MHz I.F. signal goes through lowpass filter C13, L5, and C14 to Q3 where it is amplified 18 dB. This signal then goes through FL2, an eight-pole crystal filter, which provides high selectivity (adjacent channel rejection).

2.05 The I.F. signal continues on to U7 which performs four functions:

- a) It converts the 10.7 MHz I.F. to a new 455 kHz I.F.
- b) It limits and demodulates the FM signal.
- c) It amplifies the demodulated (VF) signal.
- d) Provides a dc output voltage proportional to the receive signal level to provide audio squelch control.

2.06 Among the major ancillary components associated with U7 is crystal Y3 (pins 18 and 19) which provides the reference for the U7 oscillator. This oscillator frequency is mixed in U7 with the 10.7 MHz I.F. to produce the new 455 kHz I.F. signal. Filter FL5 provides additional filtering (pins 12, 13, 14, and 16). Potentiometer R86 (pins 1 and 2) adjusts the VF output level at the front panel connector. The two outputs of U7 are the squelch voltage (pin 10) and the audio output (pin 3).

3. SQUELCH

3.01 The squelch voltage from U7 passes through R95 (SQUELCH ADJ)

on the front panel and is amplified by U8(A) and U8(B). The level can be monitored at the white RX LEVEL test point on the Receiver module front panel (normally +2 to +7 Vdc). The output of U8(A) also goes to comparator U10(A) which is used to control the FET audio switch, U9. During normal operation (the receive level measured at J4 RX IN is above -115 dBm), the output of U10(A) is a logic "1" (+9 Vdc), and the FET switch allows the audio signal from U7, pin 3 to pass from its input at U9, pin 1 to the U9, pin 2 output going to U11. If the receive level is at or below -115 dBm, the U10(A) output drops to 0 Vdc and U9 blocks the audio output.

3.02 Comparator U10(B) and switch Q13 drive the RX SIGNAL LED DS2. The green LED is "ON" when the receive level is above -115 dBm, and "OFF" when the signal is below -115 dBm. The squelch voltage also goes to comparator U10(C) whose output is 0 Vdc (un-squelched) or +13 Vdc (squelched). This Squelch Out voltage at J1, pin 9 is sent to either the Interface or Combiner module (whichever is used in this Terminal).

3.03 During normal operation, the U9, pin 2 output is amplified by U11. It is then filtered by the 6 kHz lowpass filter composed of C112, C113, C114, and L26, and output to J1, pin 6 (AUDIO OUT) at -10 dBm, 600 ohms (unbalanced). The signal is then sent to the Combiner module for Receiver audio output combining and selection.

4. LOCAL OSCILLATOR

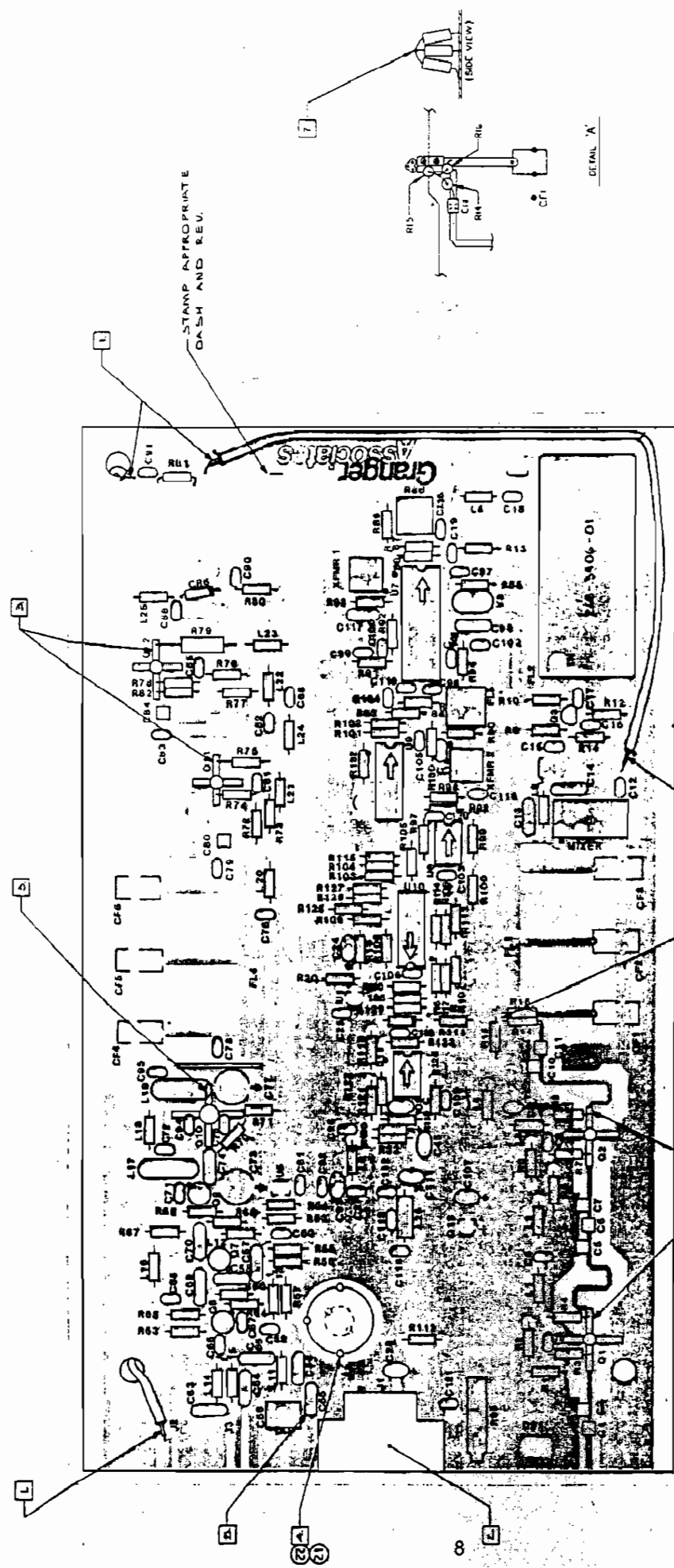
4.01 The reference local oscillator (L.O.) for both the Transmitter and Receiver is comprised of Q7 and its associated circuitry. The reference crystal for the oscillator is selected from the frequency pairs listings in the Scancom Systems Manual. At the Master, the crystal is placed in an oven for temperature stability. The Q7 output signal goes to amplifier Q8 and to a two stage X10 Multiplier consisting of Q9 and Q10.

4.02 The L.O. signal is amplified by Q8 through a lowpass filter composed of C63, C64, C65, L14, and L15. This output goes to J3 on the front panel (LO FREQUENCY). A frequency counter is connected to J3 while C56 (LO FREQ) is adjusted to set the L.O. frequency of 90 - 100 MHz.

4.03 The L.O. signal is multiplied by Q9 and Q10 while bandpass filter FL4 removes any harmonics. This signal is then amplified by a microstrip design two-stage filter consisting of Q11 and Q12 and associated circuitry. This output is equally divided by a microstrip power divider. The divider output goes to the receiver mixer (MXR1) to downconvert the RF signal. A second output goes through J2 (LO OUT on the front panel), and through external cabling to the Transmitter Module (J2) at a +7 dBm (nominal) level.

4.04 RF diode CR6 converts the L.O. signal to a proportional DC voltage which is input to comparator U10(D). Under normal L.O. operation, the voltage at pin 8 will be +13 Vdc (logic "1"). When the L.O. power decreases by 6 dB or more, the voltage at pin 8 will drop to 0 Vdc (logic "0"). The voltage is connected to either the Interface Module or the Combiner by external cabling to provide a "Low L.O. Output Level" indication to the Terminal's alarm circuitry.

2 3 4 5 6



COMPONENT SIDE (PL. ASSEMBLY)

8. INSTALL ALL CAPS AS CLOSE TO THE BOARD AS POSSIBLE OBSERVING NORMAL WORKMANSHIP PRACTICES.
7. INSTALL R14, R15, R16 (AFTER DRAG SOLDER) VERTICALLY PER DETAIL 'A'. PROTAL, TRIM AND SOLDER (HIPPED FASHION) OPPOSITE END (TOP).
6. RESISTORS 2, 4, 7, 8, 74, 75, 76, 72, 82, TO BE INSTALLED AT FEED THRU PADS ONLY; OPPOSITE END INSTALLED AS SECOND OPERATION.
5. CSP IS FACTORY SELECT DURING TEST.
4. INSTALL SOCKETS AFTER WAVE SOLDER (S.P.C.S.)
3. TRIM COLLECTOR LEAD TO 5/32 INCH. (LONGEST LEAD IS COLLECTOR.)
2. ALIGN FLANGE OF J1 PARALLEL TO EDGE OF PCB BEFORE SOLDERING.
1. DO NOT INSTALL C1, C2, C3, C6, C7, C8, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100. DO NOT INSTALL R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, R58, R59, R60, R61, R62, R63, R64, R65, R66, R67, R68, R69, R70, R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97, R98, R99, R100.

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DRAWN BY		DATE	