MT-3 RADIO SYSTEMS

VHF AMPLIFIER INSTRUCTION MANUAL

VT-3

29 - 50 MHz

Covers Models: VT-3H040 Amplifier

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NOTE:

The user's authority to operate this equipment could be revoked through any changes or modifications not expressly approved by Daniels Electronics Ltd.

The design of this equipment is subject to change due to continuous development. This equipment may incorporate minor changes in detail from the information contained in this manual.

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1 GENERAL

1.1 Introduction

The VT-3H040 Amplifier provides the final stage of RF amplification and filtering for the VT-3H040 and VT-3H040 Transmitters. The amplifier operates over one of two distinct frequency ranges; either 29 to 38 MHz or 38 to 50 MHz, depending on which of the two lowpass output filters is installed. The output power is set to 3.0 Watts by means of an externally accessed control. The VT-3H040 Amplifier is housed in a machined aluminum case that ensures optimum RF shielding, provides a good ground, and also acts as a heatsink.

Additionally, the VT-3H040 Amplifier is equipped with output power and VSWR sensing lines which can be individually configured as open collector or linear outputs. The internal VSWR sensor protects the amplifier from high antenna VSWR by approximately halving the amplifier's RF gain when a VSWR overload condition is present.

Output filtering for the VT-3H040 Amplifier is provided by the Output Lowpass Filter Board. The Output Lowpass Filter Board is mounted in a separate compartment of the amplifier case in order to provided maximum attenuation of harmonic and other spurious signals.

Refer to Section 4.4 "VT-3H040 Amplifier Schematic Diagram" for the amplifier and Section 4.2 for the Output Lowpass schematic diagram.

1.2 Performance Specification

Type:	MT-3 series VHF Amplifier module.
Compatibility:	MT-3 series Transmitter Main Board, OS-3H040 Synth.
Frequency Range:	29.0 MHz to 38.5 MHz or 37.5 MHz to 50.0 MHz.
RF Power Output:	3.0 Watts Fixed (± 1.5 dB with temperature and supply voltage).
RF power Input:	nominal level adjustable from +4 dBm to +10 dBm, held within +/- 2 dB of nominal.
Output Impedance and VSWR:	50 Ω, Type N connector; 3:1 max. VSWR.
Input /Output Isolation:	> 60 dB
Duty Cycle:	100%: Continuous operation from -30˚ C to +60˚C (optional -40°C to +60°C)

Harmonic Emissions:	Greater than 80 dB below the carrier.
Spurious Emissions:	Greater than 90 dB below the carrier.
Transmitter Mismatch Protection:	20:1 VSWR at all phase angles.
Transmitter Alarm:	Forward power sense and reverse VSWR; - open collector output (separate or 'OR'ed configuration); -linear output (separate lines only).
Operating Temperature Range:	-30˚ C to +60˚ C, optional -40˚ C to +60°C temp test.
Operating Humidity:	95% RH (non-condensing) at +25˚ C.
Operating Voltage:	+13.8Vdc Nominal (range +11 to +16Vdc), +9.5Vdc Regulated.
Amplifier Transmit Current:	0.7 Amp typical; 1.1 Amp maximum
Amplifier Standby Current:	less than 0.5 mA.
Amplifier Enable:	Active to ground.
Amplifier Enable Response:	typically overdamped, rising to within 90% of full power within 5 msec; maximum (underdamped) overshoot of 30%.

2 THEORY OF OPERATION

2.1 Amplifier Operation

A power control circuit monitors the RF output power as sampled by a dual directional coupler and maintains a constant forward power level regardless of variations in ambient temperature, RF input level and voltage of the unregulated (nominally +13.8Vdc) supply. An externally accessible control allows adjustment of the forward power level in order to correct for any departure from the 3.0 Watt rating of the amplifier. In order to minimize harmonic emission, the RF power level is monitored at the input of the low pass filter; as a consequence, the inherent VSWR of the filter will cause the power output of the amplifier to be somewhat dependent on the VSWR presented by the load. It is therefore recommended that the VSWR presented to the output of the amplifier be less than 2:1.

The power for RF amplification is derived from the +13.8Vdc supply line. The regulated +9.5Vdc line operates the bias, control and alarm circuits associated with the amplifier. Both the +13.8Vdc and +9.5Vdc lines may be continuously connected to the amplifier; the VT-3H040 Amplifier will not draw significant current (greater than 1 mA) until the enable (ENA) line is grounded.

The RF isolation between the input and output port is high (greater than 60 dB) when the enable line is high, provided the 13.8Vdc supply line is energized. In a typical application, the enable line is not grounded until the RF input to the amplifier is stable in frequency and amplitude. This prevents unwanted spurious emissions during transmitter start-up.

2.2 Power Requirements

The current drawn from the +9.5Vdc supply should not exceed 15 mA. Current consumption of the +13.8Vdc line is dependent on transmitter frequency, temperature and supply voltage and can range from 400 mA to 1100 mA (although typical values range from 600 mA to 900 mA). The current drawn from the +13.8Vdc supply should not exceed 1100 mA under normal circumstances and should never be allowed to exceed 1500 mA.

2.3 RF Circuitry

The RF circuitry consists of a driver and final amplification stage (based on the RF power MOSFET transistors, Q1 and Q2 respectively), a dual directional coupler (made up of XFMR1 and XFMR2) for power sampling and an output lowpass filter. The lowpass filter determines the operating frequency range of the VT-3H040 amplifier. The driver stage (which includes the input attenuator / matching network R1, R7 and R53) requires a nominal drive level of approximately 9 dBm (although the range 7 to 11 dBm will provide for satisfactory performance in most cases) in order to provide the required 26 dBm level for the final amplifier. The gain of the driver stage, and hence the required input power level, may be further adjusted by changing the idle (no RF) current of Q1. This adjustment is made with R5 that is accessed by removing the cover of the amplifier case. This adjustment is factory pre-set to result in an externally (R48) adjustable output power of 3.0 Watt for a specified input level (usually that of the companion synthesizer) and is, under ordinary operation, not changed.

The final amplifier stage is comprised of Q2 and is capable of providing a maximum RF power of 3.0 Watts over the entire 29 to 50 MHz frequency range, depending on drive level, supply voltage, idle current, etc. The gate bias, which is supplied through R4 (measured at test point TP6), is controlled by the Automatic Power control (APC) circuitry to maintain a constant RF power output from the amplifier. Transformer XFMR3 isolates the RF from the +13.8 Volt supply line to the final amplifier as well as providing an impedance match between Q2 and the (nominally) 50 Ω output line. The RF blocking choke, L4, determines the maximum allowable current for the 13.8V supply line.

A 20 dB dual directional coupler, made up of XFMR2 and XFMR1, monitors the forward (XFMR2) and reverse (XFMR1) output power. The sampled power is passed through a lowpass filter (to remove harmonic power content) to detectors D1 and D2 for forward and reverse power respectively. The forward detector output is fed to the APC circuitry and forward power alarm while the reverse detector output provides an input to the reverse power alarm and overload shut down circuitry.

The final step in the RF path is output filtering and, as discussed earlier, this is done by either one of two Output Lowpass filters.

2.3.1 VT-3H040 Lowpass Filter

The VT-3H040 Output Lowpass Filter is a 50 ohm, 9 pole, reciprocal filter (L1 - L4 and C1 - C4) with a 3 dB cutoff frequency of approximately 40 MHz for the low band model and 53 MHz for the high band model. The lowpass filter assembly attenuates the desired signal's harmonics as well as any other out-of-band emissions so that a 'clean' RF signal is output to the antenna connector. Although the high band model will operate below 38 MHz, such operation is not recommended, as excessive second harmonic emission will result. The low band model will operate up to about 38.5 MHz and should be used to straddle the two bands in the vicinity of 38 MHz if required.

2.4 Power Control Circuitry

The VT-3H040 Amplifier employs a closed loop power control which uses a sample of the forward RF power to control the gain of Q2 (in the final amplifier). Op-amp U4a compares the sampled RF voltage to the output power setpoint (R48) and generates an error signal which controls the voltage, applied to the gate of Q2. The RF gain of Q2 increases with the voltage applied to the gate. The output power setpoint is determined by R48, the Output Power Adjust potentiometer.

Op-amp U4b and diode D3 form a voltage limiter that prevents the gate voltage applied to Q2 from exceeding the maximum level set by the "Final Current Limit Adjustment" (potentiometer R42). The voltage limit is required to prevent Q2 from drawing excessive current (damage level) from the 13.8V supply under conditions of zero or low RF input. If the 9.5V supply is enabled when no RF is present, the APC will increase the voltage applied to the gate of Q2 until some voltage approaching 9.5V is reached and, if no voltage limiter was present, such a high gate voltage would cause damage level current to be drawn through inductor L4 and Q2.

Op-amp U1a serves as a buffer between the voltage limiter and the gate circuitry of Q2. The bypass capacitors, C11 and C10, and R40 have a time constant associated with them that will affect the settling time of the APC. The APC settling time determines the turn on time of the power amplifier. The time from transmitter enable to 90 % RF power is approximately 5 ms. Other relevant time constants are C33, R46 of the control loop and R51, R5, C3 and C2 of the driver stage.

The forward power is sampled by XFMR2 and D1. The power control circuitry keeps the output power of the amplifier constant with temperature, supply voltage, and RF input level. Since the power is sampled before the Lowpass Filter, impedance variations of the filter with frequency will cause the RF output level of the amplifier to be somewhat frequency dependent.

2.5 Power Sensing Circuitry

The VT-3H040 Amplifier is equipped with output power and VSWR sensing lines which can be individually configured as open collector or linear outputs. In open collector configuration, the output is active low, that is, when a fail condition is detected (not enough output power or too high antenna VSWR) the open collector transistor is turned on. In linear configuration, a voltage proportional to the sensed output power or antenna VSWR is output.

Both the Output Power Alarm setpoint and the VSWR Alarm setpoint are individually adjustable; however, the Output Power Alarm setpoint must always be adjusted before the VSWR Alarm setpoint. This is because the Output Power Alarm setpoint is used as a reference by the VSWR Alarm circuitry.

2.5.1 Output Power Sense

The output power sense circuitry uses directional coupler XFMR2 to sample some of the forward power (-20 dB sample). The sampled power is passed through a filter consisting of L7, L5, C38, and C21, is then rectified by diode D1 and, finally, amplified by op-amp U2a. The gain of op-amp U2a is controlled by R16, the output power alarm adjust potentiometer. The amplified voltage is then output directly in linear operation (JU1 installed, JU2 not installed) or compared to a 4.75 Volt reference by op-amp U1b, which then drives transistors Q5 and Q6 for open collector operation (JU1 not installed, JU2 installed).

In open collector configuration, Q6 (the open collector output transistor) is turned on when an alarm condition occurs. The adjustment range for the output power alarm can vary depending on the setting of R16 (the Output Power Alarm Adjust potentiometer).

2.5.2 VSWR Sense

The VSWR sense circuitry uses directional coupler XFMR1 to sample some of the power reflected from the antenna terminal. The reflected power is passed through a filter consisting of L6, L8, C39 and C22, rectified by diode D2, and then amplified by op-amp U3a. The gain of op-amp U3a is controlled by R28, the VSWR Alarm Adjust potentiometer. The amplified voltage is then output directly in linear operation (JU4 installed, JU3 not installed) or compared to the output power alarm setpoint (one-half the output of U2a) by op-amp U2b which then drives transistor Q7 for open collector operation (JU4 not installed, JU3 installed).
In open collector configuration, Q7 (the open collector output transistor) is turned on when an alarm condition occurs. The adjustment range for the VSWR Alarm can vary, depending on the setting of R28 (the VSWR Alarm Adjust potentiometer).

2.5.3 VSWR Overload

The VSWR overload circuit protects the VT-3H040 Amplifier from excessive antenna VSWR by reducing the amplifier's gain (output power) when an overload condition occurs. The VSWR overload circuit (R50, R29, R37, R38, R39, U3b, and Q8) is an extension of the VSWR sense circuit and operates in a similar manner to the VSWR sense open collector circuit. The VSWR Overload Adjust potentiometer (R29) adjusts the voltage level of the VSWR Alarm Setpoint. The voltage set by R29 is the compared to the output power alarm setpoint by op-amp U3b which then drives transistor Q8. When transistor Q8 turns on, signaling an overload condition, resistor R50 is grounded which reduces the output power setpoint. Reducing the output power setpoint lowers the gain, and hence, current drawn by the VT-3H040 Amplifier. This action protects the amplifier from overheating due to the excessive current draw that results from high antenna VSWR.

The VSWR overload circuit's range of adjustment depends on the setting of the VSWR Alarm Adjust potentiometer (R28). The VSWR overload transistor Q8 can be activated at the same point at which the VSWR alarm becomes active or the VSWR overload circuit can be disabled by turning R29 completely counterclockwise.

3 VT-3H040 AMPLIFIER ALIGNMENT

3.1 General

Connections to the power supply, alarm and transmit enable lines (ENA), are clearly marked on the amplifier case. The amplifier is enabled when the enable line (ENA) is grounded.
If the amplifier is installed in the transmitter, alignment is simplified by using an SR-3 Subrack, SM-3 System Monitor, and RF extender cable to provide transmitter power and signal interconnection (see the Transmitter Main Board Manual for details). For complete transmitter alignment refer to the VHF Enhanced Transmitter Instruction Manual VT-3H 29 - 50 MHz (IM20-VT3H040).

If the input RF level is not changed, adjustments to the output power and alarm thresholds may be made without removing the amplifier cover. However, in the case of a complete amplifier alignment, the amplifier should be separated from the Transmitter Main Board and the amplifier cover removed to expose all amplifier circuitry. All jumpers and test points are clearly marked.

3.2 Repair Note

The VT-3H040 Amplifier is mainly made up of surface mount devices which should not be removed or replaced using an ordinary soldering iron. Removal and replacement of surface mount components should be performed only with specifically designed surface mount rework and repair stations complete with Electrostatic Dissipative (ESD) protection.

When removing Surface Mount Solder Jumpers, it is recommended to use solder braid in place of manual vacuum type desoldering tools when removing jumpers. This will help prevent damage to the circuit boards.

3.3 Recommended Test Equipment List

Alignment of the transmitter requires the following test equipment or its equivalent.

Dual Power Supply:	Regulated +9.5Vdc at 0.1A.
	Regulated +13.8Vdc at 2A - Topward TPS-4000
Oscilloscope / Multimeter:	Fluke 97 Scopemeter
Current Meter:	Fluke 75 multimeter
Radio communications test set :	Marconi Instruments 2955R
VSWR 3:1 mismatch load:	JFW 50T-035-3.0:1
coaxial test cable set	three 50 Ω cables of incremental length 20 to 40 cm
Alignment Tool:	Johanson 4192

3.4 Printed Circuit Board Numbering Convention

To ease troubleshooting and maintenance procedures, Daniels Electronics Limited has adopted a printed circuit board (PCB) numbering convention in which the last two digits of the circuit board number represent the circuit board version. For example:

- PCB number 43-912010 indicates circuit board version 1.0;
- PCB number 50002-02 indicates circuit board version 2.0.

All PCB's manufactured by Daniels Electronics are identified by one of the above conventions.

3.5 Standard Factory Settings and Jumper Configuration

The VT-3H040 Amplifier is factory configured as follows:

- Open collector configuration for Output Power Alarm.
- Open collector configuration for Antenna VSWR Alarm.

The corresponding jumper settings are:

• Jumper JU1:	not installed	Output power alarm - linear output
• Jumper JU2:	installed	Output power alarm - open collector output
• Jumper JU3:	installed	Antenna VSWR alarm - open collector output
• Jumper JU4:	not installed	Antenna VSWR alarm - linear output
• Jumper JU5:	installed	Automatic Power Control (APC) enabled

3.6 VT-3H040 Amplifier Alignment

3.6.1 General

The VT-3H040 Amplifier is a frequency sensitive module that is factory assembled to operate in one of two frequency bands: 29 to 38 MHz or 38 to 50 MHz. The amplifier is normally provided with an input power level of 7 to 11 dBm. The amplifier output power level is set to 3.0 Watts by means of an externally accessed output power adjustment. The driver idle current adjustment, R5 is preset at the factory to maintain constant output power for a given range of input power levels and is one of two factory settings that are accessed with the amplifier cover removed. The second adjustment is the final current limit adjustment, R42, and this should not be changed unless the final amplifier transistor, Q2, is replaced during a repair operation.

The VT-3H040 Amplifier provides Output Power and Antenna VSWR Alarm outputs which can be configured for open collector output or linear operation. The amplifier's output power level and alarm levels can be set without detaching the amplifier from the transmitter board. However, to change the configuration of the output power alarm or the Antenna VSWR alarm, the VT-

3H040 Amplifier must be detached from the MT-3 Transmitter Board. Refer to Section 4.3, "VT-3H040 Amplifier Component Layout" for the location of solder jumpers JU1 to JU5.

3.6.2 VT-3H040 Amplifier Adjustment

The Amplifier alignment consists of two adjustment procedures; (i) a general set up (section 3.6.2.1) procedure, which sets up the proper bias conditions for the RF transistors, and (ii) the RF threshold adjustments, which set up the desired alarm threshold levels as well as the RF output power. The general alignment procedure is required following major repair operations, changes in RF input levels or large changes in operating frequency (greater than ± 1.0 MHz).

The RF output and alarm threshold level adjustments are more easily accessible so that fine adjustments can be made in the field. Depending on user requirements, the RF alarm threshold levels should be checked whenever a significant change in operating frequency (± 0.5 MHz) is made. As the antenna VSWR alarm is dependent on the output power alarm, the output power alarm should always be set first. The order of adjustment should be:

1) Set the desired output power alarm level (section 3.6.2.2).
2) Set the desired output power level (section 3.6.2.3).
3) Set the desired Antenna VSWR alarm level (section 3.6.2.4).
4) Set the desired overload condition level (section 3.6.2.5).
5) Procedure Verification (section 3.6.2.6).

Details for the alignment steps are outlined below.

3.6.2.1 General Set-Up

All of the setup steps detailed below are performed at the factory as part of the initial Transmitter alignment. A general realignment of the Amplifier Module will be required under the following conditions:

(i) the nominal RF input power applied to the amplifier is changed from that which the amplifier was initially set up for, and
(ii) components, particularly the RF transistors Q1 and Q2, are replaced during a repair operation.

The amplifier gain varies with frequency so that steps (8) through (12) should at least be checked if a large change in frequency (1 MHz or greater) is made. Moreover, if the intended channel range covers more than 1 MHz in bandwidth, steps (8) through (12) should be checked at the extreme channel limits. Steps (3) and (7) are only required if the final transistor, Q2, or the circuitry associated with the bias of Q2 is changed during a repair operation.

CAUTION: Do not apply power to the amplifier until step 6

1. Connect the transmitter's antenna output connector to the type N input of the radio communications test set through a short section of low loss 50 Ω coaxial cable.

2. Turn the 'output power adjustment', R48 and 'forward output alarm adjustment', R16, *fully clockwise*.

3. Turn the 'final current limit adjustment', R42, *fully counterclockwise*.

4. Turn the remaining (3) adjustment potentiometers (R5, R28, R29), *fully counterclockwise*.

5. Remove the RF connection to the input of the amplifier or at least assure that *no RF input is applied*.

> **CAUTION:** Make sure that R5 and R42 are fully counterclockwise before applying the 13.8 Volt supply. Failure to do so may result in destruction of one or both of transistors Q1 and Q2. (If it is known that R42 is already set it can be left in its present state). If in doubt set R42 counterclockwise and include steps (3) and (7) in the alignment.

6. Apply power (no RF input is applied) to the amplifier and enable transmitter (PTT on transmitter or "ENA" grounded on the amplifier case).

7. Monitor the 13.8Vdc supply current and adjust R42, the final current limit adjustment, so that approximately 900 mA is being drawn on the +13.8Vdc line.

8. The driver idle current is the difference between the total current drawn by the 13.8V line and the current limit as set in the previous step, *with no RF input applied*. The driver idle current must be between 5 mA and 100 mA. If, for example, the current limit was set to exactly 900 mA in step 7, the total current drawn by the 13.8V line will range from 905 mA to 1000 mA. Increase (turn clockwise) the 'driver idle current adjustment', R5, until the total 13.8V line current rises slightly (about 5 to 10 mA) above the initial 900 mA limit set in step (7). This is the minimum driver idle current setting. While counting turns of the adjustment, slowly increase R5 (Driver Idle Current) until the total current is 1000 mA. Take note of this position for the next step and then *return R5 to just below the minimum current (5 to 10 mA) position*.

9. Apply RF power to the input of the amplifier at the level expected in normal room temperature operation. Slowly increase R5 until either; (1) the power output of the amplifier no longer increases significantly ('flattens out') as the adjustment is turned or; (2) the maximum driver idle current setting (determined from the approximate position of R5 as recorded in step (8)) is reached. Do not exceed this amount by very much or damage may occur. If the power output is less than 4.0 Watts, corrective action must be taken.

10. Select the most preferred (i.e. closest to the top) maximum power setting from Table 3-1 that is closest to the amplifier output level, and then readjust R5 to match this power level. A power level of 4.5 or 5.0 Watts would be ideal; a power level of 4.0 Watts is the minimal requirement.

11. Turn the 'output power adjustment', R48, fully counterclockwise. The power output from the amplifier should be under one of the values in the minimum power column of table 3-1. If the output power is greater than 1.0 Watt then return the 'output power adjustment', R48, to its maximum value (clockwise) and repeat steps 10 and 11 until the best match to an entry closest to the top of table 3-1 can be found. If no setting of R5 can bring the minimum output power under 1.5 Watt while drawing a minimum driver idle current of approximately 5 mA, corrective action must be taken.

12. Remove the RF input to the amplifier and note the driver idle current. This current should be between 5 mA and 100 mA. If it is significantly beyond this range, corrective action must be taken. If the settings approach marginal conditions as exemplified by the values in the bottom row of table 3-1, steps 8 through 12 may be repeated in an effort to improve overall performance. The objective is to find a setting for R5 that results in the maximum power adjustment range while keeping the driver idle current significantly above 5 mA. Maximizing amplifier performance while keeping this objective is obtained by adopting settings closest to the top of Table 3-1. Table 3-1 is intended to serve only as an adjustment guideline and actual settings of the amplifier may be an interpolation of the values listed.

13. Once adjustment of R5 is complete, the RF input power may once again be applied to the amplifier.

Table 3-1 Suggested Tuning States for the PA

Suggested tuning states (top to bottom in decreasing preference). A supply voltage of 13.8 Volt is assumed. This table is intended to serve only as a guideline to aid in adjustment. Actual settings may be interpolated from the values listed.

Minimum Output Power [Watts]	Maximum Output Power [Watts]	Driver Idle Current (no RF input) [mA]	Performance Rating
under 0.5	5.0	10 to 60	very good
under 0.5	4.5	10 to 60	very good
under 1.0	4.5	10 to 60	good
under 1.0	5.0	10 to 100	good
under 0.5	4.5	60 to 100	good
under 1.0	4.5	5 to 100	fair
under 1.0	4.0	10 to 100	fair
under 1.5	5.0	5 to 10	fair
under 1.5	4.0	20 to 60	fair
under 1.0	4.0	5 to 10	marginal
under 1.5	4.0	5 to 100	marginal

3.6.2.2 Output Power Alarm (Forward Power)

Open Collector Output

Note: the output power alarm output is factory configured as an open collector output so a pull-up resistor may be required on the amplifier 'FOR' alarm pin (transmitter pin B26) if one is not already present.

1. Adjust R48, the 'output power adjustment', to the output power at which the Output Power Alarm is to be activated, usually 1.5 Watt.

2. Monitor the Output Power Alarm pin ('FOR' or B26), and slowly turn R16, the 'output power alarm adjustment', counterclockwise until the pin goes low. The alarm is now set for the current output power of the transmitter.

Linear Output

1. Open the amplifier case to disable (open circuit) jumper JU2 and enable (short) jumper JU1.

2. Monitor the Output Power Alarm pin ('FOR' or B26) with a voltmeter.

3. Adjust R48, the 'output power adjustment', for full transmitter output power (3 Watts).

4. Adjust R16, the 'output power alarm adjustment', so that the voltmeter indicates +7.5Vdc for full transmitter output power.

5. Turn R48, the 'output power adjustment', fully counterclockwise. The voltmeter should read approximately +3Vdc.

6. Disconnect the voltmeter.

3.6.2.3 Output Power

1. Turn R48, the 'output power adjustment', clockwise to the desired transmitter output power.

3.6.2.4 Antenna VSWR Alarm (Reverse Power)

Open Collector Output

> **Note:** the antenna VSWR alarm output is factory configured as an open collector output so a pull-up resistor may be required amplifier 'REV' alarm pin (transmitter pin Z26) if one is not already present. The output power alarm must be set first before the antenna VSWR alarm can be set.

1. Disconnect the radio communications test set and terminate the transmitter with the 3:1 mismatch load. Couple the transmitter output to a spectrum analyzer through a minimum 10dB attenuation (to protect analyzer input) and monitor spectrum output ensuring spectral purity. Spurs must be smaller that –60dBc.

2. Monitor the Antenna VSWR Alarm pin (amplifier pin REV, transmitter pin Z26), and turn R28 fully counterclockwise. The alarm output pin should be high. Slowly turn R28 clockwise until the 'REV' pin or Z26 pin is pulled low.

3. *Slowly* turn R28 counterclockwise until the point where the 'REV' pin or Z26 pin is once again high. (Stop turning R28 immediately after the 'REV' pin returns to high.)

4. Reconnect the 3:1 mismatch load with another cable that is 20 to 40 cm longer than the previous cable.

5. Monitor the Antenna VSWR Alarm pin (amplifier pin 'REV', transmitter pin Z26). If the alarm output pin is pulled low, slowly turn R28 counterclockwise until the 'REV' pin or Z26 pin is once again high; otherwise (if the alarm pin remained high) leave R28 unchanged.

6. Repeat steps (4) and (5) with yet another cable.

7. Connect a 2:1 mismatch load and verify that the 'REV' pin remains high for all three cable lengths used in steps 1 through 6. Confirm any spurs that exist are smaller than –60dBc.

8. Put the 50 ohm load back on again, the 'REV' pin or Z26 pin should remain high. The reverse power trip point is now set for a VSWR of 3:1 (or slightly above). Confirm any spurs that exist are smaller than –60dBc.

1. Disconnect any loads attached to transmitter and monitor spectrum confirming that any spurs are smaller than –60dBc. If spurs are greater than the expected value, adjust the Driver Idle Current in Section 3.6.2.1 to a minimum of 5mA and a maximum of 15mA. If any driver idle current adjustments are made, repeat all tests from Section 3.6.2.1 to confirm correct operation.

   Note: The VSWR alarm setting is somewhat dependent on operating frequency due to the inherent RF characteristics of the Lowpass Output filter. If the threshold levels are critical, they should be checked if changes in excess of 0.5 MHz are made to the amplifier's operating frequency. Always set the VSWR alarm with the cable length that minimizes (more counterclockwise) the setting of R28.

   Technical tip: If the cover to the amplifier is removed, the reverse alarm set-up procedure discussed above may be simplified by monitoring the voltages at test points, TP9 and TP10 (see the component layout in section 4.3). When the amplifier is producing 3 Watt into a *matched termination*, the measured voltage at TP10 should be 0.5 to 1.5V. If the voltage at TP9 is less than 1/50 that of TP10 (with a matched termination) then only a single cable is required to set the VSWR alarm thresholds as discussed above. Multiple cables are required if the voltage at TP9 is greater than 1/50 but less than 1/5 that of TP10 (with a matched termination). Corrective action should be taken if the voltage at TP9 is greater than 1/5 that of TP10 (with a matched termination). The alarm thresholds are set with the cable that results in the highest voltage at TP9, when the amplifier is connected to a *mismatched load having a 3:1 VSWR.*

Linear Output

1. Open the amplifier case to disable (open circuit) jumper JU3 and enable (short) jumper JU4.

2. Monitor amplifier pin 'REV' or transmitter pin Z26 with a voltmeter.

3. Disconnect the radio communications test set and terminate the transmitter with the 3:1 mismatch load.

4. Adjust R28, the VSWR alarm adjustment, so that the voltmeter indicates +5Vdc for a 3:1 mismatch.

5. Repeat step (4) for two to three cables of lengths increasing in increments of 20 to 40 cm. Select the cable that minimizes (more counterclockwise) the setting of R28.

6. Put the 50 ohm load back on again. The voltmeter should read under 2Vdc.

7. Disconnect the voltmeter.

3.6.2.5 Antenna VSWR Overload

1. Disconnect the radio communications test set and so that the amplifier is terminated with an open circuit.

2. Monitor the current from the +13.8Vdc supply.

3. Adjust R29, the 'VSWR overload adjustment', clockwise until a noticeable drop in the +13.8Vdc current occurs.

4. Repeat step (3) using two to three cables of lengths increasing in increments of 20 to 40cm. Select the cable that minimizes (more counterclockwise) the setting of R29.

5. Check the +13.8Vdc current with an open circuit condition for all three of the cables. The current should not exceed 800 mA in any case. If the current exceeds 800 mA for any cable, corrective action should be taken.

6. Reconnect the radio communications test set and; the +13.8Vdc current should return to the normal operating level and the output power should be 3.0 Watt.

3.6.2.6 Procedure Verification

1. Verify that the current drawn from the +13.8Vdc supply is less than 1.0A and from the +9.5Vdc supply is less than 0.02A when transmitting full RF output power (3 Watt). If the current drawn from the +13.8Vdc supply exceeds 1.0A at room temperature, the amplifier should be tested at supply voltages and ambient temperatures expected in the field to assure that the current never exceeds 1.1 Amps.

2. Turn off the power to the transmitter.

4 ILLUSTRATIONS AND SCHEMATIC DIAGRAMS

4.1 VT-3H040 Output Lowpass Filter Component Layout

Do not print this page.
Replace this page with Page 1, Section 1 of
"VT3040AMP 11x17 pages".

4.2 VT-3H040 Output Lowpass Filter Schematic Diagram

4.3 VT-3H040 Amplifier Component Layout

Do not print this page.
Replace this page with drawing VT3AMPM1.
(VT3AMPM1 Amp CLD 43-932611)
Layers:
Instruction Manual
TH Hi Pwr
TH Lo Pwr Dsgn
TH Lo Pwr Parts
SM Hi Pwr Dsgn
SM Hi Pwr Parts
SM Lo Pwr Dsgn
SM Lo Pwr Parts
BARE BOARD

4.4 VT-3H040 Amplifier Schematic Diagram

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(VT3AMPM2A AMP Sch V1.1)

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Replace this page with Page 2, Section 2 of
"IM21-VT3150AMP 11x17 pages".

5 PARTS LISTS

5.1 VT-3H040 Amplifier Electrical Parts List

Ref Desig	Description	Part No.
C1	CAP., SM, 10nF CER., 1206, X7R	1008-4B103K5R
C2	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C3	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C4	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C5	CAP., SM, 1nF CER,0805,X7R,50V	1008-3A102K5R
C6	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C7	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C8	CAP., SM, 1.0uF TANT., 20%,35V	1055-5B105M35
C9	CAP., SM, 1nF CER., 1206, C0G	1008-3B102K1G
C10	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C11	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C12	CAP., SM,43pF PORCEL.,5%,500V	1036-1B2430J5
C13	CAP., SM, 1nF PORCEL., 10%,50V	1036-3B2102K0
C14	CAP., SM, 1nF CER,0805,X7R,50V	1008-3A102K5R
C15	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C16	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C17	CAP., SM, 10uF TANT., 10%, 35V	1055-6D106K35
C18	CAP., SM,120pF PORCEL.,5%,300V	1036-2B2121J3
C19	CAP., SM, 10uF TANT., 10%, 35V	1055-6D106K35
C20	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C21	CAP., SM, 56pF CER., 0805, C0G	1008-1A560J1G
C22	CAP., SM, 56pF CER., 0805, C0G	1008-1A560J1G
C23	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C24	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C25	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C26	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C27	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C28	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C29	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C30	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C32	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C33	CAP., SM,47nF CER,0805,X7R,50V	1008-4A473K5R
C34	CAP., SM,10nF CER,0805,X7R,50V	1008-4A103K5R
C35	CAP., SM,100nF CER,0805,X7R,50	1008-5A104K5R
C36	CAP., SM, 1nF CER., 1206, C0G	1008-3B102K1G
C37	CAP., SM, 1nF CER,0805,X7R,50V	1008-3A102K5R
C38	CAP., SM, 56pF CER., 0805, C0G	1008-1A560J1G
C39	CAP., SM, 56pF CER., 0805, C0G	1008-1A560J1G
D1	DIODE, MMBD701,HOT CARR.,SOT23	2105-MMBD7010
D2	DIODE, MMBD701,HOT CARR.,SOT23	2105-MMBD7010
D3	DIODE, BAS16, SWITCHING, SOT23	2100-BAS16000
D4	DIODE, MBZ5233B,6.0V ZEN.SOT23	2102-MBZ5233B
FB1	FERRITE BEAD, 73MIX,3x3.5mm OD	1210-73030350
FB2	FERRITE BEAD, 73MIX,3x3.5mm OD	1210-73030350

Ref Desig	Description	Part No.
J1	CONN., SMB, JACK,2 HOLE FLANGE	5120-J2SC01BG
L1	INDUCTOR, SM, 390nH, 10%, 1812	1255-2GR3900K
L2	CHOKE, RF/MOLDED,680nH,10%,.37	1251-2B00R68K
L3	CHOKE, RF/MOLDED,680nH,10%,.37	1251-2B00R68K
L4	CHOKE, RF/MOLDED,680nH,10%,.37	1251-2B00R68K
L5	INDUCTOR, SM, 390nH, 10%, 1812	1255-2GR3900K
L6	INDUCTOR, SM, 390nH, 10%, 1812	1255-2GR3900K
L7	INDUCTOR, SM, 390nH, 10%, 1812	1255-2GR3900K
L8	INDUCTOR, SM, 390nH, 10%, 1812	1255-2GR3900K
LPF1	FILTER, EMI, Pi/5500PF,8-32UNC	1302-P552D10D
LPF2	FILTER, EMI, Pi/5500PF,8-32UNC	1302-P552D10D
LPF3	FILTER, EMI, Pi/5500PF,8-32UNC	1302-P552D10D
LPF4	FILTER, EMI, Pi/5500PF,8-32UNC	1302-P552D10D
LPF5	FILTER, EMI, Pi/5500PF,8-32UNC	1302-P552D10D
PCB	PCB, AMPLIFIER, VT-3/040 TX	4320-15500332
Q1	CAP SCREW, M3x6 HEX SOCK-M2.5	5816-3M0SH06S
Q1	POLYFET, F2246,2W SINGLE ENDED	2043-F2246000
Q2	CAP SCREW, M3x6 HEX SOCK-M2.5	5816-3M0SH06S
Q2	POLYFET, F2247,4W SINGLE ENDED	2043-F2247000
Q3	MOSFET, NDS352AP,P CHAN,SOT-23	2142-NDS352AP
Q4	MOSFET, NDS352AP,P CHAN,SOT-23	2142-NDS352AP
Q5	TRANSISTOR, BC817-25,NPN,SOT23	2120-BC817025
Q6	TRANSISTOR, PZT2222A,NPN,ST223	2120-PZT2222A
Q7	TRANSISTOR, PZT2222A,NPN,ST223	2120-PZT2222A
Q8	TRANSISTOR, BC817-25,NPN,SOT23	2120-BC817025
R1	RES., SM, 75R0 1206, 1%,100ppm	1150-1B75R0FP
R2	RES., SM, 1K00 1206, 1%,100ppm	1150-3B1001FP
R3	RES., 22R METAL FILM, 5%, 0.5W	1101-1A0220JP
R4	RES., 100R METAL FILM, 5%,0.5W	1101-2A0101JP
R5	POT., SM, 10K, 12T, TOP ADJUST	1172-M30103W5
R6	RES., SM, 49K9 0805, 1%,100ppm	1150-4A4992FP
R7	RES., SM, 100R 1206, 1%,100ppm	1150-2B1000FP
R8	RES., SM, 27K4 0805, 1%,100ppm	1150-4A2742FP
R9	RES., SM, 18R2 0805, 1%,100ppm	1150-1A18R2FP
R10	RES., SM, 18R2 0805, 1%,100ppm	1150-1A18R2FP
R11	RES., SM, 100R 0805, 1%,100ppm	1150-2A1000FP
R12	RES., SM, 100R 0805, 1%,100ppm	1150-2A1000FP
R13	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R14	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R15	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R16	POT., SM, 50K, 12T, SIDE ADJ.	1172-M30503X5
R17	RES., SM, 4K53 0805, 1%,100ppm	1150-3A4531FP
R18	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R19	RES., SM, 27K4 0805, 1%,100ppm	1150-4A2742FP
R20	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R21	RES., SM, 49K9 0805, 1%,100ppm	1150-4A4992FP

Ref Desig	Description	Part No.
R22	RES., SM, 49K9 0805, 1%,100ppm	1150-4A4992FP
R23	RES., SM, 49K9 0805, 1%,100ppm	1150-4A4992FP
R24	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R25	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R26	RES., SM, 4K53 0805, 1%,100ppm	1150-3A4531FP
R27	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R28	POT., SM, 100K, 12T, SIDE ADJ.	1172-M40104X5
R29	POT., SM, 50K, 12T, SIDE ADJ.	1172-M30503X5
R30	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R31	RES., SM, 27K4 0805, 1%,100ppm	1150-4A2742FP
R32	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R33	RES., SM, 49K9 0805, 1%,100ppm	1150-4A4992FP
R34	RES., SM, 49K9 0805, 1%,100ppm	1150-4A4992FP
R35	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R36	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R37	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R38	RES., SM, 221K 0805, 1%,100ppm	1150-5A2213FP
R39	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R40	RES., SM, 1K00 0805, 1%,100ppm	1150-3A1001FP
R41	RES., SM, 100K 0805, 1%,100ppm	1150-5A1003FP
R42	POT.,SM/4mmSQ,50K,MULT/TRN,TOP	1174-DM3503W0
R43	RES., SM, 27K4 0805, 1%,100ppm	1150-4A2742FP
R44	RES., SM, 4K53 0805, 1%,100ppm	1150-3A4531FP
R46	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R47	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R48	POT., SM, 50K, 12T, SIDE ADJ.	1172-M30503X5
R49	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R50	RES., SM, 10K0 0805, 1%,100ppm	1150-4A1002FP
R51	RES., SM, 4K53 0805, 1%,100ppm	1150-3A4531FP
R52	RES., SM, 27K4 0805, 1%,100ppm	1150-4A2742FP
R53	RES., SM, 100R 1206, 1%,100ppm	1150-2B1000FP
R54	RES., SM, 100K 0805, 1%,100ppm	1150-5A1003FP
R55	RES., 47R METAL FILM, 5%, 0.5W	1101-1A0470JP
R56	RES., 47R METAL FILM, 5%, 0.5W	1101-1A0470JP
U1	IC, MC33172, DUAL OP AMP, SO-8	2302-33172N08
U2	IC, MC33172, DUAL OP AMP, SO-8	2302-33172N08
U3	IC, MC33172, DUAL OP AMP, SO-8	2302-33172N08
U4	IC, MC33072, DUAL OP AMP, SO-8	2302-33072N08
XFMR1	TRANSFORMER, TWIN N: 9.5T VHF	1293-H1029400
XFMR2	TRANSFORMER, TWIN N: 9.5T VHF	1293-H1029400
XFMR3	XFMR/TOROID, 11:13,T44-17 CORE	1290-991113FK

5.2 VT-3H040 Lowpass Filter Electrical Parts List

Ref Desig	Description	Part No.	VT-3H035	VT-3H045
C1	CAP., SM,120pF PORCEL.,5%,300V	1036-2B2121J3		●
	CAP., SM,150pF PORCEL.,5%,300V	1036-2B2151J3	●	
C2	CAP., SM,180pF PORCEL.,5%,300V	1036-2B2181J3		●
	CAP., SM,220pF PORCEL.,5%,200V	1036-2B2221J2	●	
C3	CAP., SM,180pF PORCEL.,5%,300V	1036-2B2181J3		●
	CAP., SM,220pF PORCEL.,5%,200V	1036-2B2221J2	●	
C4	CAP., SM,180pF PORCEL.,5%,300V	1036-2B2181J3		●
	CAP., SM,220pF PORCEL.,5%,200V	1036-2B2221J2	●	
C5	CAP., SM,120pF PORCEL.,5%,300V	1036-2B2121J3		●
	CAP., SM,150pF PORCEL.,5%,300V	1036-2B2151J3	●	
L1	INDUCT/TOROID, 8T,22AWG,T44-17	1290-99080022		●
	INDUCT/TOROID,10T,22AWG,T44-17	1290-99100022	●	
L2	INDUCT/TOROID, 9T,22AWG,T44-17	1290-99090022		●
	INDUCT/TOROID,11T,22AWG,T44-17	1290-99110022	●	
L3	INDUCT/TOROID, 9T,22AWG,T44-17	1290-99090022		●
	INDUCT/TOROID,11T,22AWG,T44-17	1290-99110022	●	
L4	INDUCT/TOROID, 8T,22AWG,T44-17	1290-99080022		●
	INDUCT/TOROID,10T,22AWG,T44-17	1290-99100022	●	
PCB	PCB, LPF,VT-3/150,UT-3/400 AMP	4321-16931712	●	●

5.3 VT-3H040 Amplifier Mechanical Parts List

Description	Part No.	Qty.
CASE, MT-3 VHF/UHF AMPLIFIER	3702-66102130	1
LID, CASE, MT-3 AMPLIFIER,ALUM	3702-66102151	1
SCREW, M2 X 4, PAN/PHILLIPS,A2	5812-2M0PP04S	3
SCREW, M2 X 6, PAN/PHILLIPS,A2	5812-2M0PP06S	2
SCREW, M2.5 X 6, PAN/PHIL., A2	5812-2M5PP06S	5
SCREW, M3 x 8, PAN/PHIL, A2	5812-3M0PP08S	7
SET SCREW, M3x3, HEX SOCKET,A2	5817-3M0AC03S	1
TUBING, TFE-260C,24AWG T/W,CLR	7610-260C24TW	4 x 7mm
TURRET TERMINAL, 4-40,.188L,Tn	5053-144M188T	1
WIRE, PVC/STRAND., 22AWG, RED	7110-22S07302	14cm
WIRE, PVC/STRAND., 22AWG,BLACK	7110-22S07300	10.5cm
WIRE, PVC/STRAND., 22AWG, ORG.	7110-22S07303	9.5
WIRE, PVC/STRAND., 22AWG, RED	7110-22S07302	13.5cm
WIRE, PVC/STRAND., 22AWG, BLUE	7110-22S07306	10cm
WIRE, PVC/STRAND.,22AWG,YELLOW	7110-22S07304	9.5cm
WIRE, PVC/STRAND., 22AWG,BROWN	7110-22S07301	10cm

6 REVISION HISTORY

Issue	Date	Description
1	May 97	First Issue.
2	June 97	Included PCB version 2 component layouts and schematics
3	Mar 03	Corrected wire gauge of the inductors on the lowpass filter parts list. Corrected lengths of the red PVC wire required for assembly. Corrected Typing Mistake on Component Layout: R1=75R0, R7=100R0 ECO# 575: New Ferrite Bead: Was 64 MIX, Now 73 MIX. ECO# 694: Corrected quantity of M2x4, pan/phil screws. ECO# 699: High level, unfiltered audio was coupling with the low level signal close to the output of the Audio Processor (not in this manual). The following changes were required to the Amplifier Board: Changed C20 on Amplifier Board, was 100nF, now 10nf ECO# 737 Added steps in amplifier alignment to check for spurious emissions with 3:1, 2:1, and open circuit loads.

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