Drake UV-3 Transceiver Interface

The following instructions and schematics provide the details on interfacing the Drake UV-3 tri-band VHF/UHF FM transceiver with any Advanced Computer Controls repeater controller or ShackMaster 100. While the staff at ACC doesn't have first hand experience with the UV-3, we've developed this application note based on information supplied by customers. As always, we must assume that you understand the operation of your transceiver, as described in its technical manual. We also assume that you've read and understand how your ACC controller interfaces to remote base transceivers in general.

The first part describes the basic hookup of audio, COS, and PTT for fixed frequency operation. The second part describes frequency control. The third section discusses band select techniques.

It is assumed that the UV-3 is fully functional. The Control Head will be removed, and signals will be connected to the 44 pin connector on the body of the transceiver. Several signals are alternately available at the Auxiliary (Accessory) connector.

For reference, the pinout of the Accessory connector (P1501) and the Control Head connector are shown below in Figures 1 and 2. In addition, the Control Head schematic and a schematic of those components which must be added *in place of* the removed Control Head are shown in Figure 3.

Figure 1 - Accessory Connector

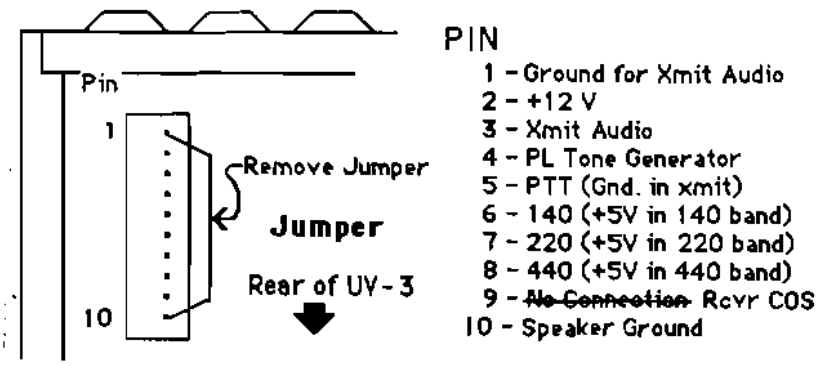

Figure 2 - Control Head Connector Pinout

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+12 Volts Switched	12	10 KHz Dial 2	A	Volume Control	N	100 KHz Dial 8
2	Dial Selected	13	10 KHz Dial 1	B	+12 V Input to On/Off Sw.	P	+Offset
3	440	14	X Offset	C	140	R	10 KHz Dial 8
4	MHz Dial 4	15	Y Offset	D	220	S	Z Offset
5	MHz Dial 2	16	Signal GND to Vol. & Sq.	E	Channel 1	T	Scan to Dial
6	MHz Dial 1	17	Scan to Channel 4	F	Audio to Vol. and Sq.	U	+ to Channel Switch
7	100 KHz Dial 4	18	Scan L.E.D.	H	Channel 2	V	+5 KHz
8	Channel 3	19	+5 Volts	J	Channel 4	W	S Meter
9	MHz Dial 8	20	Squelch Control	K	Simplex	X	Low Power (tie to ground)
10	100 KHz Dial 1	21	Mic. Audio	L	100 KHz Dial 2	Y	0 V = PTT
11	10 KHz Dial 4	22	Mic. Ground	M	-Offset	Z	GND to lamps, meter, etc.

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Drake UV-3 Transceiver Interface

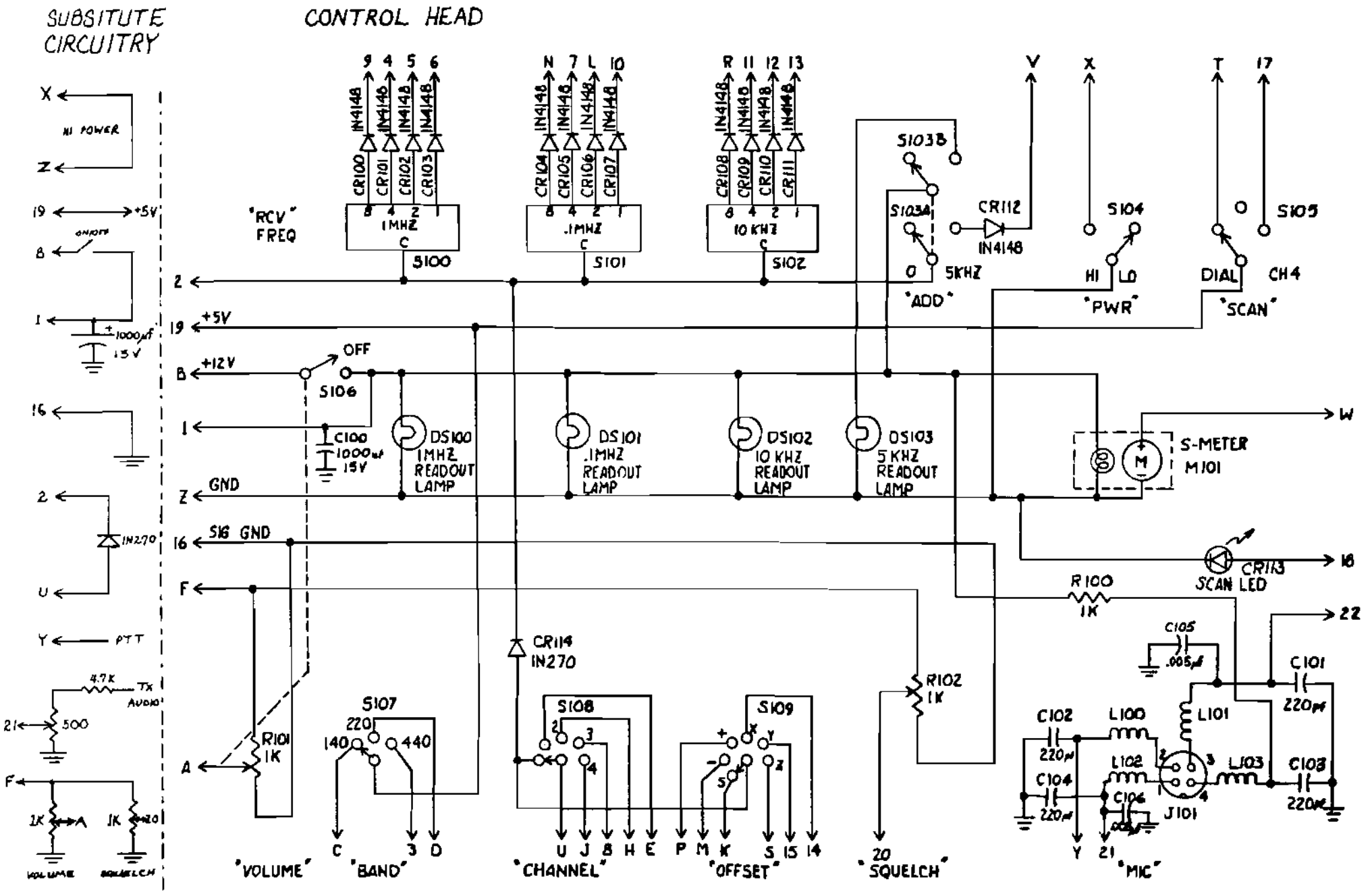


Figure 3 - Control Head Schematic and Substitute Circuitry

Frequency Control

All of ACC's repeater and remote base control products supply remote base frequency information in the form of a serial data stream which may be captured externally in a chain of shift register ICs. The data as supplied is essentially in the form required by the UV-3. Since the UV-3 logic operates at +5 volts, the shift register chain (Figure 6) should be powered by +5 volts which may be obtained from the Control Head connector, pin 19.

Simple circuitry is required to develop the "- offset" signal (Figure 6). Connect the outputs of the first pair of shift registers and the - offset logic to the Control Head connector.

With the *RC-850 controller*, this arrangement places the UV-3 at the Link/Remote Base 1 position. It may be placed on Link/Remote Base 2 by connecting the signals from the third and fourth shift registers, instead.

Note that each of the logic signals which drive the transceiver is buffered with a transistor emitter follower. This was done to ensure adequate drive current for the internal logic. A higher drive capability than available from the 4094B shift registers would be available from the 74HC164 shift register. With this part, it should be possible to eliminate the buffer transistors and base resistors, although *we have not tried it*. The two parts have different pinouts - Figures 7 and 8 show the pinout of the 4094B and 74HC164 shift registers. The 74LS04 and 74LS08 inverter and AND gate may also be replaced with 74HC04 and 74HC08 devices. Be sure to tie any unused CMOS *inputs* to ground or 5 volts - don't leave them open.

Band Select

RC-850 Controller. Band select information is available from the *RC-850 controller* data stream, commanded by the user level "Band Select" command. It's also stored in macro sets, for automatic loading by the scheduler, and in Link Memories.

The band select bits are obtained from the fifth and sixth shift registers in the chain. A one-of-eight decoder (three line to eight line demultiplexer) provides an active signal for each band which may be selected. The 2M, 220 MHz, and 440 MHz signals are supplied to the Control Head connector, pins C, D, and 3, respectively.

Other Controllers. Band select information is not available directly, but any general purpose remote control outputs may be used for band selection. One and only one of the three band select inputs at the Control Head connector must be taken high.

The *ITC-32 board* provides several "group outputs", in which several outputs may be commanded simultaneously with a single command. These outputs, with a decoder as shown for the RC-850 controller, would be well suited to band selection.

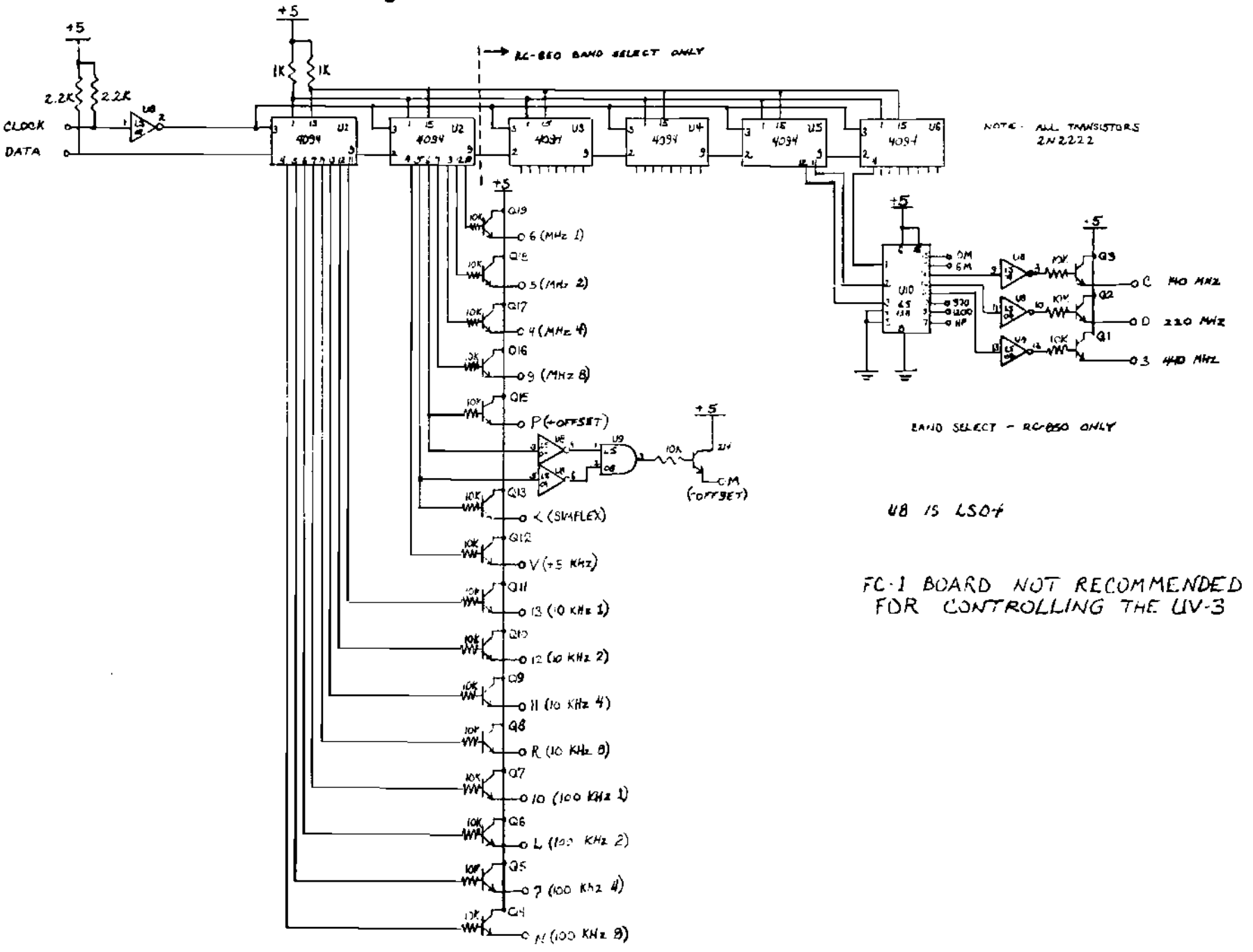
Parts Sources

Many of the required parts are available from Jameco Electronics, 1355 Shoreway Rd., Belmont, CA 94002, (415) 592-8097, and Digi-Key Corporation, P.O. Box 677, Thief River Falls, MN 56701-0677, (800) 344-4539.

Acknowledgements

We'd like to thank Jerry Clark, K7KZ, and Tom Workman, KØTW, for submitting the information used in this application note.

Figure 6 – Frequency Control Circuitry



Basic Interface

The four signals needed to/from the UV-3 are:

* Transmitter audio
* Transmitter PTT
* Receiver audio
* Receiver COS

Transmitter audio and **PTT** are available at the Accessory Connector, the 10-pin connector located on the bottom of the UV-3. The pins are numbered 1 through 10 with Pin 1 located at the end toward the front of the UV-3. Transmit audio may be taken through a potentiometer for level adjustment to pin 3 of the Accessory connector. The controller's PTT output may connect to pin 5 .

Alternately, **transmit audio** and **PTT** may be taken to the microphone input at the control head connector, with PTT applied to pin Y, and transmit audio (through a potentiometer) to pin 21. See Figure 3 for the pot.

Receiver audio is available at the SPKR phono jack on the rear of the rig. The jumper from Accessory connector pins 1 to 10 must be removed to disable the internal speaker. (While receive audio is available at the Control Head connector pin F, audio at this point has not yet been de-emphasized, and is not recommended.)

COS from the receiver should be brought out from the inside of the transceiver and be buffered to avoid loading the receiver's circuitry. The unbuffered signal may be brought to Pin 9 of the Accessory connector, as it is a spare pin and should not now be connected to anything. (Be sure it's not before proceeding.)

A 3-inch wire should be added inside the bottom cover of the UV-3 to bring out the signal. Refer to Figure 4 to help find the location for the wire.

1. Lay the UV-3 up-side down with the front of the rig toward you.
2. Remove the bottom cover and the paper covering the parent board.
3. See Figure 4 to locate pin 3 of the offset board connector on the parent board. Carefully solder one end of the wire to that pin.
4. Route the wire to the right along the existing wire bundle to pin 9 of the P1501 accessory connector.
5. Solder the remaining end of the wire as far down on pin 9 as possible to avoid interference when mating the Accessory connector.
6. Replace the paper over the parent board and reinstall the bottom cover.

This COS signal is not capable of interfacing directly to the controller because it would load the receiver's high impedance circuitry. A small op amp circuit must be added externally to buffer the signal (Figure 5). The op amp is used as a comparator to allow adjustment of the COS threshold. This adjustment permits the COS logic signal to "track" the squelch quieting threshold inside the receiver.

A "high true" COS is supplied to the controller. The RC-85 controller and the ITC-32 board require a high true link COS signal. The RC-850 controller and ShackMaster should be set for high true COS.

Note: +12 V and ground are available at the Accessory and Control Head connectors.

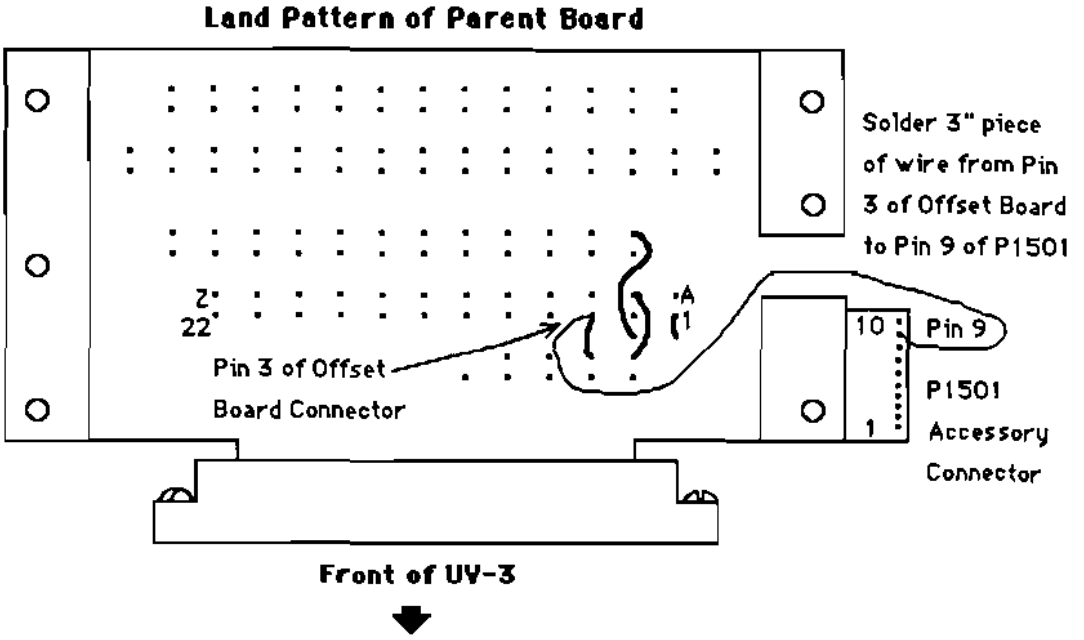


Figure 4 - Unbuffered COS Signal Location

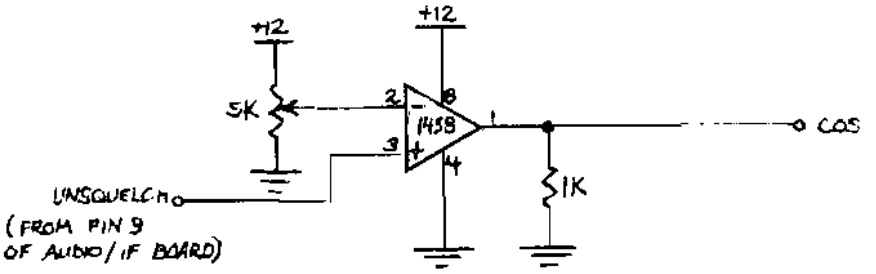


Figure 5 - COS Buffer Circuit

National Semiconductor

microCMOS

MM54HC164/MM74HC164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HC164/MM74HC164 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-Bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-Bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

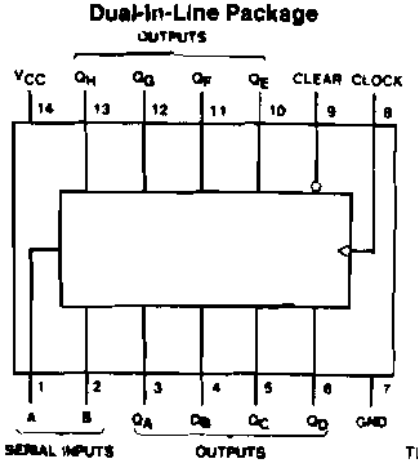
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 19 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: $< 1\ \mu A$
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

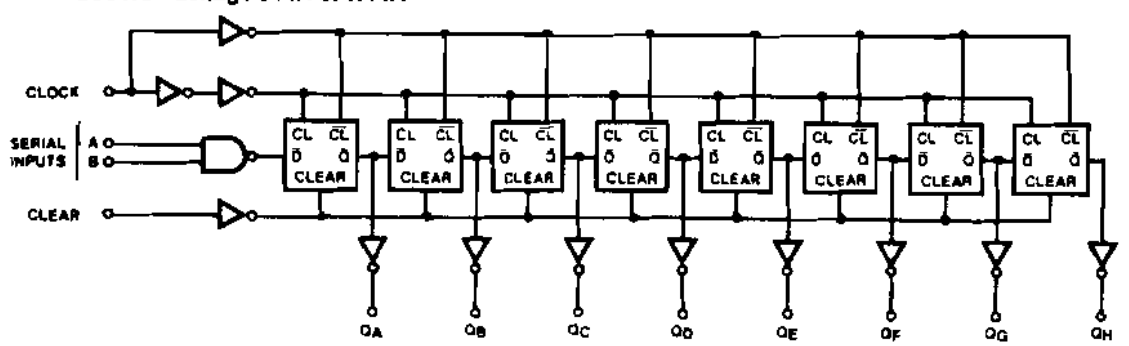
Dual-In-Line Package



TL/F/5315–1

Top View

Order Number MM54HC164J or MM74HC164J,N
See NS Package J14A or N14A



TL/F/5315–2

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Figure 8 - 4094B Data Sheet

National Semiconductor

CD4094BM/CD4094BC 8-Bit Shift Register/Latch with TRI-STATE® Outputs

General Description

The CD4094BM/CD4094BC consists of an 8-bit shift register and a TRI-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_S) can be used to cascade several devices. Data on the Q_S output is transferred to a second output, Q'_S, on the following negative clock edge.

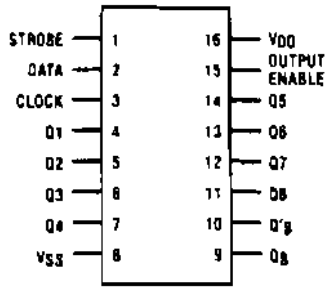
The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is high, data propagates through the latch to TRI-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken high.

Features

■ Wide supply voltage range	3.0 V to 18V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ TRI-STATE outputs	

Connection Diagram

Dual-In-Line Package



Order Number CD4094BMJ or CD4094BCJ
See NS Package J16A

Order Number CD4094BMN or CD4094BCN
See NS Package N16E

Block or Logic Diagram